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INVESTIGATION OF DEFECTS AND IMPURITIES IN SILICON-ON-SAPPHIRE.(U)
NOV 76 R A WILLIAMS, J E MAURITS, J L PEEL F19628-75-C-0108

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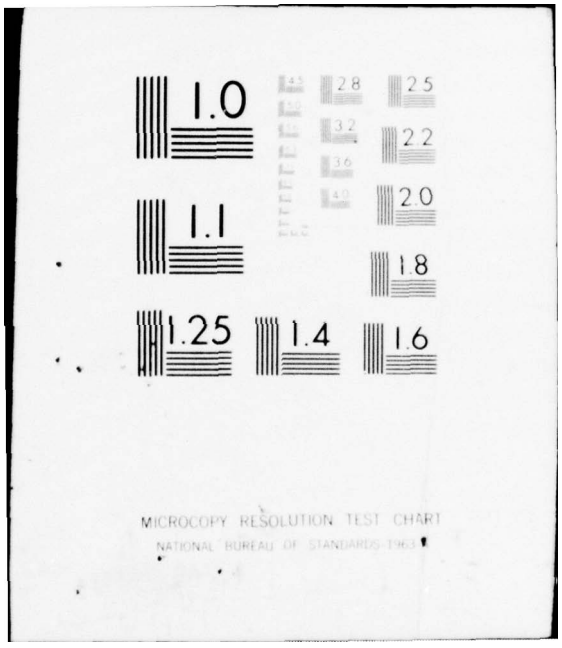
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Final Report
November 1976

INVESTIGATION OF DEFECTS AND IMPURITIES IN SILICON-ON-SAPPHIRE

Rockwell International Corporation

ROME AIR DEVELOPMENT CENTER
AIR FORCE SYSTEMS COMMAND
GRIFFISS AIR FORCE BASE, NEW YORK

Drs. Ross A. Williams, J. L. Peel, Jan E.A. Maurits and Frieda F. Mittelbach are the responsible investigators for this contract. Mr. Bobby L. Buchanan is the RADC Project Engineer.

This report has been reviewed by the RADC Information Office (OI) and is releasable to the National Technical Information Service (NTIS). At NTIS it will be releasable to the General public, including foreign nations.

This technical report has been reviewed and approved for publication.

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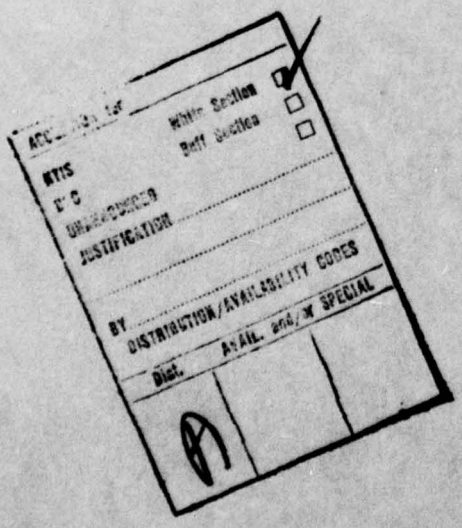

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Sapphire Polish	Integrated Circuit Yield

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

With the use of silicon-on-sapphire (SOS) in the manufacture of MOS/LSI circuitry rapidly approaching reality for military applications, the problem of nonuniform and inconsistent quality from lot-to-lot and wafer-to-wafer in commercially available SOS material must be dealt with. The first phase of this program examines the relationship between defects and impurities in the sapphire starting material and the quality of devices fabricated

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20. ABSTRACT (Continued)

in silicon films grown on the sapphire. The quality of the sapphire was examined using selective etching, X-ray topography, ion-microprobe-mass-analyzer (IMMA), and scanning electron microscope. Device quality was determined on the basis of yield, electrical parameters, and radiation hardness of CMOS inverters. Sapphire growth, sapphire polishing, and Si film growth were done by several manufacturers in different combinations, and the results of the different combinations of manufacturers compared. The results indicated that a high yield of good quality devices could be obtained on material which had earlier shown a high defect density, and that chemical impurities in the silicon film, incorporated from the sapphire during film growth, led to higher initial and post irradiation drain leakages.

The second phase of the program investigated the relationship between different pre-epitaxial treatments of the sapphire and CMOS device quality. The sapphire treatments studied were polishing, cleaning, hydrogen prefire, and pre-epitaxial annealing environments. The material for Phase II was all supplied by Union Carbide Corporation under a subcontract. The results indicated that, although p-channel transistors were not greatly affected by any of the sapphire treatments investigated:

1) reducing the amount of sapphire polish was beneficial to n-channel yield and radiation-induced leakage,

2) radiation-induced n-channel leakage is very sensitive to Si film thickness,

3) isopropyl alcohol as a final cleaning rinse is detrimental, and

4) some hydrogen prefire is beneficial to n-channel yield and radiation-induced leakage.

This report briefly summarizes the work in Phase I and describes the Phase II work in detail.

EVALUATION STATEMENT

INVESTIGATION OF DEFECTS AND IMPURITIES IN SILICON-ON-SAPPHIRE

Final Report
Rockwell International
F19628-75-C-0108

This report is the Final Report on this contract. It covers investigations relating the characteristics of silicon-on-sapphire (SOS) materials and SOS processing techniques to the quality of devices fabricated in the epitaxial silicon layers grown on sapphire during the period 15 January 1975 to 30 June 1976. The objective of this work was to delineate the SOS material selection and processing procedures that yield material from which quality, radiation hard MOS/SOS devices can be fabricated. Specific steps in polishing and cleaning sapphire substrates and pre-epitaxial heat treatment can result in improved device yields and reduction in radiation-induced leakage at the silicon-sapphire interface. The continued improvement in both yield and hardening of MOS/SOS devices is essential as LSI circuitry using the MOS/SOS technology finds increasing application in radar and communications systems.

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1. INTRODUCTION

1.1 Scope of Program

A serious problem in the development of SOS technology has been material-related problems, particularly the variations in n-channel SOS transistor leakage currents from lot-to-lot and wafer-to-wafer. The silicon-sapphire interface is thought to play a critical role in determining the uniformity of device electrical parameters and radiation hardness. The studies performed under this contract were designed to investigate the relationship between SOS material characteristics and the quality of CMOS/SOS integrated circuits.

The first phase (January 1975 to January 1976) of this contract was concerned with relating defects in SOS material to device yield and quality, while the second phase has been concerned with identifying SOS material fabrication procedures leading to improved device yield and quality. Because the first phase was described in detail in Interim Technical Report, RADC-TR-76-208, July 1976, this report covers the second phase (January 1976 to July 1976). However, a brief review of the result of the first phase is given in the following subsection, while the rest of the report deals with Phase II.

1.2 Phase I

The first phase of this study was primarily directed at determining the impact that sapphire defects and impurities have on the electrical parameters and radiation hardness of CMOS/SOS transistors. As a part of this effort, sapphire substrates were examined which were supplied by three vendors--Union Carbide, Tyco and Crystal Systems. The wafers were polished by Union Carbide, Tyco and Insaco (for Crystal Systems) with half of each group from Tyco and Crystal Systems also being polished by Union Carbide.

The sapphire substrates were examined using selective etch and X-ray diffraction topography and Ion Microprobe Mass Analysis (IMMA) techniques. The results from the first two analysis techniques are shown in Table 1-1. The results showed a wide variation in sapphire quality and surface smoothness. Of the samples evaluated, the Union Carbide sapphire appeared to have the least defects and the fewest scratches. The IMMA results for all samples showed contaminants concentrated on the surface of the sapphire, indicating that the impurities remained from the polishing and pre-silicon-deposition cleaning steps. Generally, the impurities consisted of micron-size sapphire chips and remnants of polishing compounds--with some residue left after the final cleaning rinse.

Silicon films from two different sources [Union Carbide (UC) and Hewlett Packard (HP)] were deposited on sapphire substrates from the three vendors indicated above. Each sapphire vendor type had

Table 1-1. SOS Wafer Quality

	Vendor/Polisher				
	U.C./U.C.	Tyco/Tyco	Tyco/U.C.	C.S./U.C.	C.S./Insaco
Surface Defects (H_3PO_4 Selective Etch)	10^4-10^5 cm^{-2}	10^5-10^6 cm^{-2}	10^5-10^6 cm^{-2}	10^5-10^6 cm^{-2}	10^5-10^6 cm^{-2}
Dislocation Banding (H_3PO_4 Selective Etch)	None Observed	Some Banding Observed	Some Banding Observed	Prominent Banding Observed	Prominent Banding Observed
Grain Boundaries (H_3PO_4 Selective Etch)	None Observed	None Observed	None Observed	Numerous Sites Observable	Numerous Sites Observable
Scratches (X-ray Topography)	Few Detectable	Numerous Scratches Ranging From Coarse to Very Fine	Few Detectable	None Detectable	Readily Observable Scratches -- Mainly Saw Marks
Dislocations (X-ray Topography)	10^3-10^4 cm^{-2}	10^4-10^6 cm^{-2}	10^4-10^6 cm^{-2}	10^4-10^6 cm^{-2}	10^4-10^6 cm^{-2}

two polishing variations--the vendor-furnished polish and a Union Carbide polish. Also, some experimental films were deposited by Rockwell on one group of Union Carbide sapphire wafers.

All of the silicon films were found to possess discrete inclusions of impurities, in varying degrees. These inclusions appeared vividly in surface maps generated using the IMMA technique. This particular technique has proven valuable in determining the quality of the deposited silicon film, since many of the impurities, which are observed with the IMMA, either are transparent or are too small to be observed optically. The corresponding impurity sites, however, did appear in SEM photomicrographs and were correlated with the IMMA surface maps.

The effects of impurities and crystal imperfections in silicon and sapphire upon the finished device characteristics were studied using 4007 type circuits fabricated on the SOS material using a simple, radiation-hard process procedure. Two wafers from each sapphire and polishing group were included in each device processing lot, to improve the probability of obtaining at least one processed wafer for each material variation. For the most part, this approach was successful. The electrical test data indicated that good electrical characteristics were obtainable for the various groupings of SOS material--apparently independent of sapphire substrate quality. However, the Tyco group of wafers seemed, in general, to yield below-average results, either because of the material or the processing. Tyco material polished by Tyco and having Union Carbide silicon films (Tyco/Tyco/UC) showed very poor results. This particular group showed problems on every wafer (lot 506) indicating that the silicon on these substrates may have been of poor quality. Only one wafer in the Tyco/UC/UC group was found to be good (lot 503). The Tyco/UC/HP group and the Tyco/Tyco/HP group, however, yielded satisfactory devices.

The wafer maps for leakage currents showed that all groups of material were capable of producing good CMOS/SOS circuits. The yields found on some Crystal Systems wafers, with Insaco polish showed that very high yields could be achieved on material which had earlier shown a high defect density with highly scratched surfaces; however, it appeared that devices lying along, or adjacent to, deep saw cuts tended to fail more readily than those between the saw marks.

The wafer mapping also showed that the defects were randomly distributed which tends to rule out most processing-related problems and is probably a reflection of either material problems (such as defects in silicon films serving as enhanced diffusion conduits between source-drain regions) or mask defects. To eliminate the latter variable, devices were selected which showed neither apparent processing nor mask defect problems, as evidenced by electrical probe data and optical examination. The IMMA results on these carefully chosen dice, which generally

included only one failed device among several good devices, showed no impurity inclusions. These results were very surprising. However, contamination, as found in the pre-processing surface maps, was present in the 1 mm square silicon test area on the same sample. This result was true in nearly every wafer examined, implying that impurity inclusions were removed in the device areas which went through all the processing steps. The large silicon test areas were covered with a thick silox layer during the entire processing cycle, except during two short oxidation steps.

Radiation results showed that there is no particular correlation between backchannel hardness and the gate threshold hardness. This conclusion appears to be true when comparing the Union Carbide and the Hewlett Packard silicon films as shown in Figures 1-1a and 1-1b. Devices fabricated with the Union Carbide deposition showed the best backchannel results, while the Hewlett Packard films showed the best oxide hardness with good to poor backchannel hardness.

The first phase has further verified previous observations that the silicon epitaxial films containing the highest concentrations of impurities generally produce devices with higher initial drain-leakages and higher post-irradiation leakage currents. Although wide variations were observed, even for a given wafer and film, the following qualitative statements can be made. The experimental Rockwell film (lot 505) showed the highest contamination level, as shown in Figure 1-2, and the devices fabricated in that film generally exhibited the greatest backchannel leakages. The Union Carbide film (lot 504) was the "cleanest," and the corresponding devices generally exhibited the least backchannel leakages. All other films and corresponding devices tended to be intermediate in contamination levels and leakages, respectively.

The results from this study tended to discourage the use of sapphire selective etch and X-ray topographs to determine the suitability of sapphire material for SOS use. It appears likely that the eventual quality of the silicon films will depend on the following:

- Substrate surface roughness
- Substrate surface cleanliness
- Sapphire pre-fire conditions
- Silicon deposition rates
- Silicon film uniformity

The second phase of this study was structured to address all of these areas except for the silicon deposition rates. The remainder of this final report will discuss the results of the final six months of this effort.

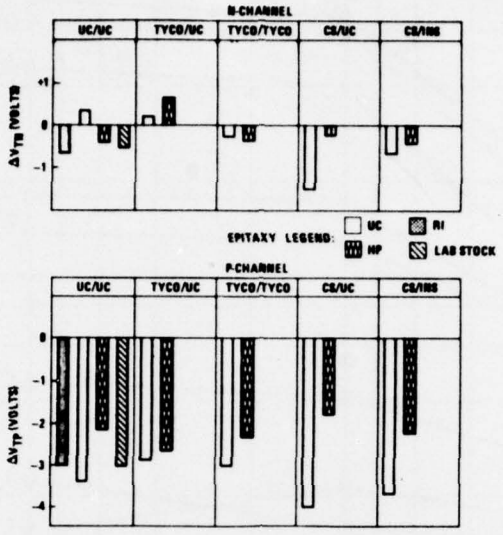

Figure 1-1a. Radiation-Induced Threshold Voltage Shift Data After 10^6 Rads(Si) and V_G = +10 Volts

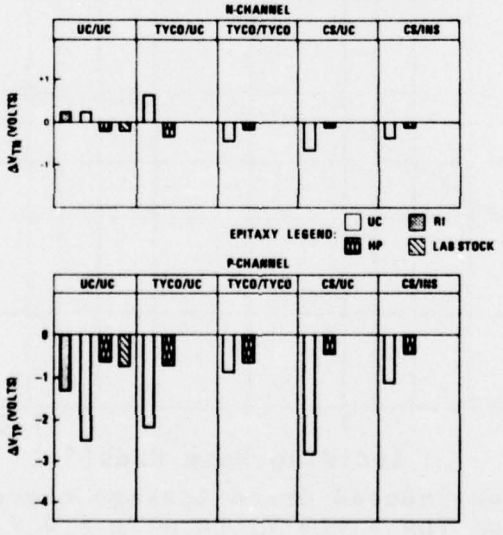

Figure 1-1b. Radiation-Induced Threshold Voltage Shift Data After 10^6 Rads(Si) and V_G = -10 Volts

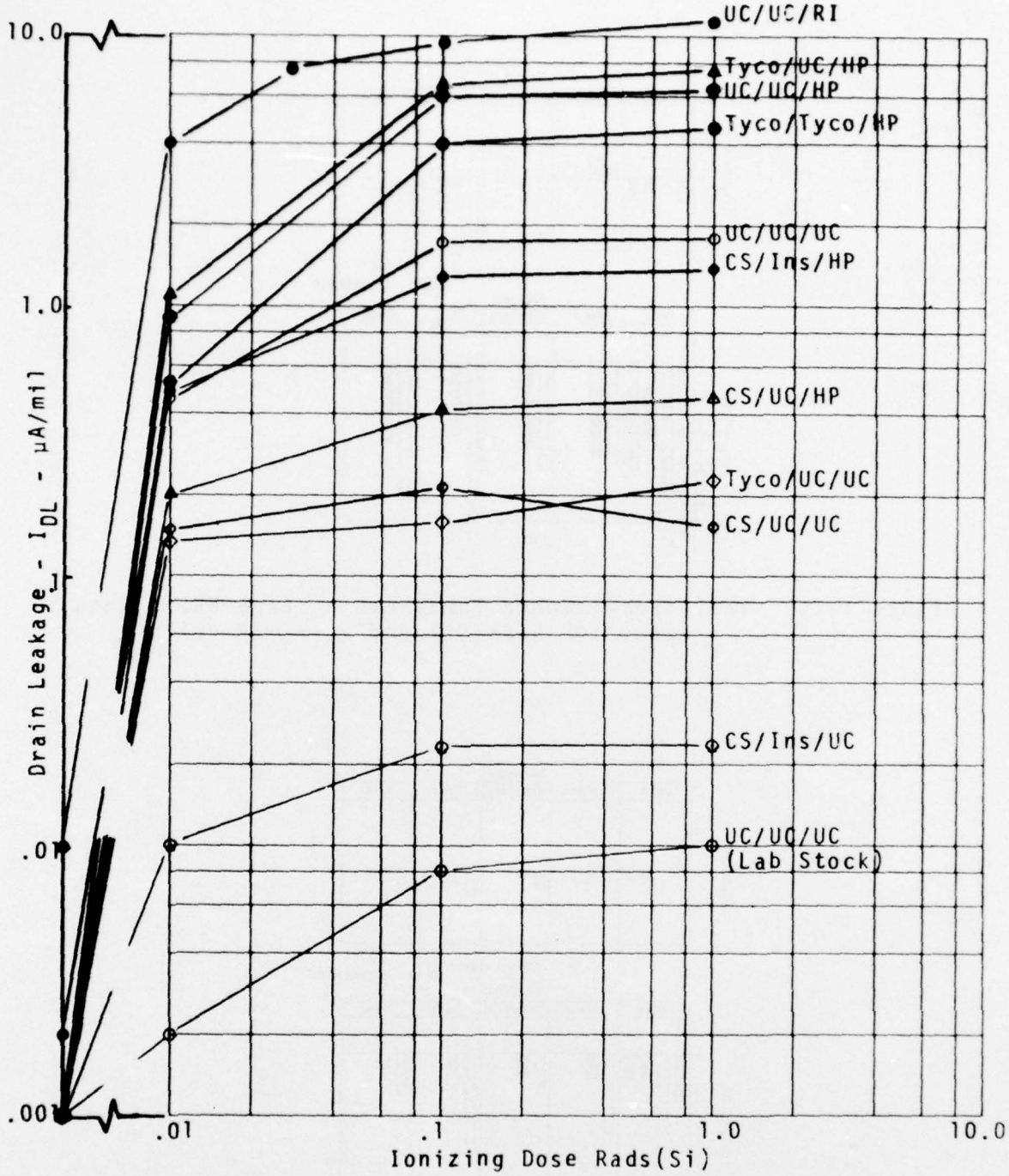

Figure 1-2. Radiation induced drain leakage current, I_{DL}, for the condition V_{DN} = +10 V, V_G = V_S = 0 V on n-channel devices fabricated on Union Carbide (UC), Rockwell International (RI), and Hewlett Packard (HP) silicon epitaxies. Each point is the average of three samples across each wafer.

1.3 Phase II

In January 1976 the Crystal Products Department of Union Carbide Corporation and Rockwell International, Autonetics Group, began a cooperative program to study the effects of various pre-epitaxial conditions on device parameters. Administratively, this cooperative program was established with Rockwell International functioning as the prime contractor and Union Carbide Corporation functioning as the subcontractor.

1.3.1 Goals

The goal of this program has been to study the effects of pre-epitaxy substrate preparation on the electrical properties of radiation-hardened CMOS devices fabricated on SOS material. For the materials section of the program, the objective was to fabricate several SOS wafer lots, representing a wide range of experimental surface conditions, in order to perform studies of effects of pre-epitaxy material quality variations on device performance. Substrate surface finish variations, chemical cleaning variations, hydrogen prefire time variations, oxygen anneal cycles, and hydrogen chloride anneal cycles were the experimental conditions studied.

1.3.2 Technical Approach

This phase of the program was concerned with fabrication of SOS wafers with process variations in pre-epitaxy conditions. The approach followed was to fabricate SOS wafers (UCC starting material) with variations in the above procedures for the pre-epitaxial treatment of the sapphire, and to build devices on these wafers (Rockwell radiation-hardened CMOS/SOS fabrication) and evaluate the resulting CMOS/SOS devices with regard to yield, electrical characteristics, stability, and radiation tolerance. A total of 100 wafers was supplied representing four experiments. The actual experimental conditions and number of wafers in each experimental lot were defined to fit device processing requirements and reflect the most recent information on critical surface quality parameters. Current reports from several SOS users and preliminary analysis and device results from Rockwell were used to refine and redesign experimental conditions as the program progressed. Table 1-2 lists the actual experimental lots and number of SOS starting material wafers fabricated for subsequent evaluation, i.e., CMOS/SOS device evaluation to identify specific areas for further detailed study and investigation. Experimental Sets I - III were variations of the standard fabrication and pre-epitaxy procedures. Set IV described new experimental conditions, which are not part of the standard fabrication or pre-epitaxy process. These experiments were designed to represent a wide range of pre-epitaxy surface conditions.

Table 1-2. Experimental Lots of SOS Starting Material

Set I. Surface Finish and Substrate Variations

Exp. Lot No.	Substrate Lot	Wafers	Exp. Conditions
1	KC0084	15	Standard
2	KC0014	5	Standard
3	KC0084 Redo	5	Standard
5a	KC0084 Select Finish	5	Standard
5b	KC00133	2	Standard
6	KC0084 Poor Finish	5	Standard

Set II. Pre-Epitaxial Chemical Cleaning Variations

7	KC0084	5	Final Alcohol Rinse
8	KC0084	5	Final Acid Clean
9	KC0084	5	Final D.I. Water Scrub

Set III. Hydrogen Prefire Conditions

11a	KC0084	5	O min. Hydrogen Prefire
11b	KC00133	7	O min. Hydrogen Prefire
12a	KC0084	5	30 min. Hydrogen Prefire
12b	KC00133	7	30 min. Hydrogen Prefire

Set IV. Annealing Experiments

16a	KC0084	5	16 hr. O_2 at 1100°C
16b	KC00133	7	16 hr. O_2 at 1100°C
17a	KC0084	5	2 min. HCl at 800°C
17b	KC00133	7	2 min. HCl at 800°C

At program start, fifty (50) wafers from two sets of experiments, variations in substrate surface finish quality, and variations in pre-epitaxy chemical cleaning were delivered to Rockwell for evaluation. Later in the program, a second delivery of 50 wafers from the remaining two sets of experiments, variations in hydrogen prefire time and experimental gaseous annealing, was made. All substrates used were ($1\bar{1}02$) orientation, 2.0 inch diameter, 0.013 inch thick, fabricated to standard specifications. The epitaxial films were approximately 0.75 microns thick, intrinsic resistivity (undoped). The SOS wafer fabrication process is outlined in Table 1-3.

On January 29, 1976, the first delivery of 50 wafers (Group I) was made. These were Experimental Lots 1, 2, 3, 5a, 6, 7, 8, and 9. All films were measured at greater than 700 ohm-centimeters resistivity. Conductivity type could not be determined. All films were grown in the same reactor, B1200, using the same silane cylinder, in contiguous runs with preprogrammed deposition times, temperatures, and flow rates. The same operator grew all of the films.

On May 6, 1976, the second delivery of 50 wafers (Group II) was made. These were Experimental Lots 5b, 11a, 11b, 12a, 12b, 16a, 16b, 17a, and 17b. All of these films were made in the A1200 reactor, a different reactor than used for the first lot. The same silane cylinder was used for all films in this lot, but a different cylinder than used for the first lot. The same preprogrammed deposition times, temperatures, and flow rates were used, except for the noted pre-epitaxy annealing and prefire experiments.

Table 1-4 summarizes the characteristics of the SOS starting material, while Table 1-5 outlines the sapphire selection for the various wafer lots.

At Rockwell, upon receipt from Union Carbide, the wafers were subjected to a visual inspection using a Nomarski interference contrast filter, examined for silicon thickness variations using a sodium light interferometer and silicon thickness measured in three places using an IR spectrophotometer. The details of this pre-processing inspection are given in Appendix A. The wafers were then divided into three processing lots for device fabrication. The first lot (lot 610) contained 12 wafers consisting of 4 wafers having all procedures standard, 4 wafers with an "inferior" sapphire polish, and 4 wafers with a "select" sapphire polish. The second processing lot (lot 618) also contained 12 wafers--4 wafers for each of the three sapphire cleaning variations. The third processing lot (lot 627) contained 20 wafers in five groups of 4 wafers each, including one group of completely standard wafers, as a control, two groups of hydrogen prefire variations, and two groups of annealing ambient variations.

The devices chosen for fabrication on the experimental SOS wafers were 4007SR CMOS inverters. The mask set used contained special

Table 1-3. Manufacturing Sequence of SOS Wafers

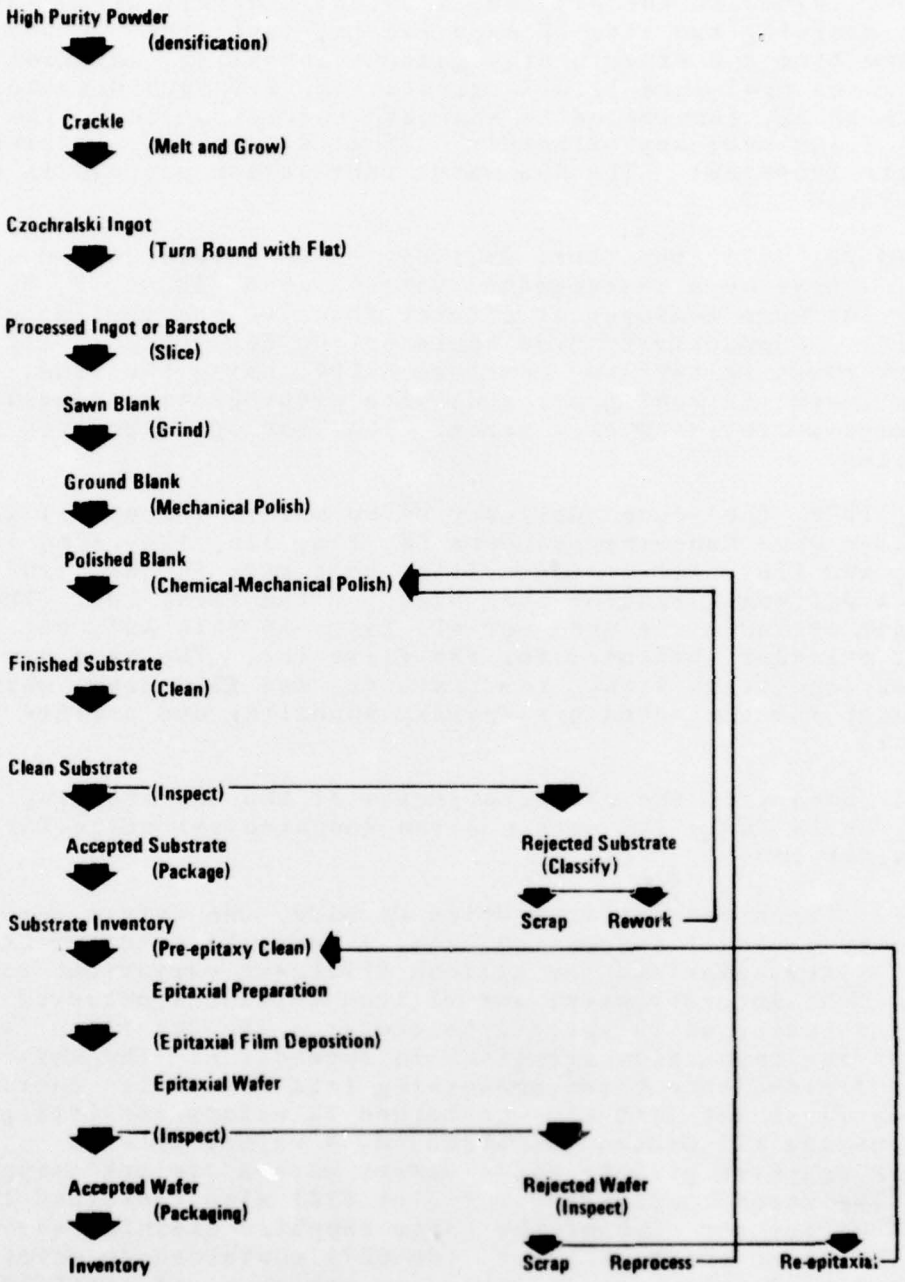

Table 1-4. Summary of SOS Starting Material

	UCC LOT NUMBER	NO. OF WAFERS	SUBSTRATE LOT	SAPPHIRE POLISH	SAPPHIRE CLEAN	PRE-EPITAXIAL ANNEAL AND/OR PREFIRE	EPITAXY RUN NUMBER
GROUP I	1	15	KC0084	Standard	Standard	Standard	B12012901 & 02
	2	5	KC0014	Standard	Standard	Standard	B12012904
	3	5	KC0084 Redo	Standard	Standard	Standard	B12012903 & B12013002
	5a	5	KC0084	Select	Standard	Standard	B12012901
	6	5	KC0084	Poor	Standard	Standard	B12012905
	7	5	KC0084	Standard	Alcohol Rinse	Standard	B12013004
	8	5	KC0084	Standard	Acid Wash	Standard	B12013001
	9	5	KC0084	Standard	Water Scrub	Standard	B12012906 B12013003
GROUP II	5b	2	KC00133	Standard	Standard	Standard	A12050605
	11a	5	KC0084	Standard	Standard	No Prefire	A12050508
	11b	7	KC00133	Standard	Standard	No Prefire	A12050603
	12a	5	KC0084	Standard	Standard	30 Min H_2 Prefire	A12050506
	12b	7	KC00133	Standard	Standard	30 Min H_2 Prefire	A12050611
	16a	5	KC0084	Standard	Standard	16 hr O_2 at 1100°C	A12050608
	16b	7	KC00133	Standard	Standard	16 Hr O_2 at 1100°C	A12050607
	17a	5	KC0084	Standard	Standard	2 Min HCℓ at 800°C	A12050609, 12
	17b	7	KC00133	Standard	Standard	2 Min HCℓ at 800°C	A12050606

Table 1-5. Flow Chart for Substrate Lot Selection

EXPERIMENTAL SETS I–IV

Select 3 Substrate Lots, each containing all substrates cut from individual, identified ingots.

Substrate Lot KC0084
Crystal No. M15-1861-9

Select 6 substrates for Experimental Lot No. 6 and repolish

Assign remaining substrates to Experimental Lots 1, 3, 5a, 7, 8, 9, 11a, 12a, 16a, 17a

Substrate Lot KC0014
Crystal No. M14-1722-27

Assign to Experimental Lot No. 2

Substrate Lot KC00133
Crystal No. M13-1899-3

Assign to Experimental Lots 5b, 11b, 12b, 16b, 17b

test devices at regular intervals among the 4007SR inverter dice. The device fabrication is described in greater detail in Appendix B. Following device fabrication, the wafers were probed and measurements made of channel leakage, output voltage under load, gate leakage, drain breakdown voltage, and turn-on threshold voltage. Yields were determined on the basis of the leakage current, output voltage, and gate leakage measurements, and the wafers were mapped with respect to location and failure mode of unacceptable devices. The details of the wafer probe measurements and yield determination are given in Appendix C. Devices selected from each wafer on the basis of wafer maps and the silicon thickness measurements were then evaluated as to radiation induced channel leakage and turn-on threshold shift in a Co^{60} environment, as described in Appendix D. Selected devices from each wafer were also evaluated under bias-temperature stress, as described in Appendix E. The four experiments--namely, sapphire polish, sapphire cleaning, hydrogen prefire, and annealing ambient--are described and the results given in the following sections, while a final section summarizes the program and gives the conclusions and recommendations.

2. SAPPHIRE POLISH EXPERIMENTS

2.1 Technical Approach and Rationale

The quality of the surface polish on the sapphire substrate is expected to have a strong effect on the quality of the silicon which is later grown on the sapphire. Surface imperfections, such as scratches will expose crystal orientations different from the desired surface orientation, leading to local variations and defects in the crystal structure of the epitaxial silicon. Also, there is a strong tendency for impurities to become trapped in scratches and other surface imperfections, where they are less likely to be removed by ordinary cleaning procedures. The association of impurities with scratches was established by IMMA analyses in Phase I of this program. The work in Phase I also established a strong correlation between silicon impurities and device quality, especially initial and radiation-induced drain leakage currents. Thus it is important to investigate the effect of sapphire polish quality on the yield and characteristics of CMOS/SOS devices.

2.2 Sapphire Substrate Preparation

As described above, the first set of experiments was designed to study variations in substrate surface quality. Substrate lot selection is shown in Table 1-5 (see Section 1.3), a flow chart of substrate lot selection and use in the experimental lots. Boule history cards (on file at UCC, Crystal Products) are used to identify each substrate lot from crystal growth through epitaxy. The card contains crystal identification as well as processing and yield information. The crystal identification number identifies the particular growth station used, date of growth, and growth data.

Substrate lot identification and substrate preparation variations for the first experimental set are given in Table 2-1.

Table 2-1. Surface Finish and Substrate Variations
Experimental Set I

Lot KC0084	Lot KC0084
Select 28 substrates and clean with standard procedure. Load into epitaxial reactor in 2 runs of 14 each. Select 5 wafers with best surface quality for Experimental Lot No. 5a. Select 15 wafers of standard quality for Experimental Lot No. 1.	Select 12 substrates and prepare for mechanical polishing. At the chemical-mechanical polishing step, separate into 2 groups of 6 each. One group of 6 shall have a 75% reduction in cycle time. The other group of 6 shall have a 50% cycle time reduction. Use standard pre-epitaxial cleaning procedure. Keeping lots separate, load into epitaxial reactor and deposit film. Select 2 wafers from 50% cycle and 3 wafers from 75% cycle for Experimental Lot No. 6.

2.3 Description of SOS Starting Material

Epitaxial run identification for the first experimental set is listed below.

Experimental Set I Identification

Experimental Lot No.	No. of Pcs.	Substrate Lot	Experimental Conditions	Epitaxial Run No.
1	15	KC0084	Standard	B12012901 B12012902
5a	5	KC0084	Select Surface Quality	B12012901
6	5	KC0084	Poor Surface Quality	B12012905

All substrates were cleaned with the standard cleaning procedure described in a subsequent section of this report. Standard epitaxial prefire conditions were used as described in a subsequent section of this report.

The epitaxial reactors used in this work are vertical rotary reactors and are made by Applied Materials, Inc., Santa Clara, California, Model AMV1200. The substrates are placed flat onto a graphite susceptor, and the susceptor is rotated to provide good wafer-to-wafer uniformity. Time, temperature and gas flows are pre-programmed to minimize operator error and maintain run-to-run uniformity. Nitrogen, hydrogen, or hydrogen chloride atmospheres can be selected as desired. Deposition of silicon results from chemical vapor decomposition of silane.

2.4 Starting Material Wafer Specifications

The standard specification for substrates and epitaxial wafers is given in Table 2-2, referenced as Union Carbide Corporation, Crystal Products Department Product Specification SOS-10. In addition to conforming to these specifications, a test for particulates was performed on the wafers. Lot samples were inspected microscopically using Nomarski interference contrast for particulates in the film. Film resistivity was intrinsic, greater than 700 ohm-cm, type indeterminate. Film thickness was held at ~0.75 micron, within the range of 0.70 - 0.80 microns for the center value. No haze was visible on any of the wafers. Particulate contamination was held to a minimum, with microscopic examination at 100X showing less than 10 particles larger than 2 microns diameter in an X-Y scan of the surface.

Substrates were standard size 2.0 inch diameter, 0.013 inch thick, with standard surface quality except where noted as an experimental condition. Experimental lot number 6 had a poor surface quality that did not meet specification, as planned for this experiment.

Table 2-2. Product Specifications*

SILICON-ON-SAPPHIRE EPITAXIAL WAFERS

Czochralski Grown Sapphire Substrates:

A. Material Specifications

1. The orientation of the substrate is $(1\bar{1}02) \pm 2^{\circ}$. Structural (hexagonal) indices.

2. The substrate flat is 45° to the projected "C"-axis of the sapphire substrate and parallel to the (110) epitaxial silicon plane.

3. The substrate is free of slips, twins or lineage.

B. Geometrical Specifications

Thickness	1.500" Diameter -	0.013" ±.002"
	2.000" Diameter -	0.013" ±.002"
	3.000" Diameter -	0.020" ±.002"
Bow	1.500" Diameter -	0.0015" max. (excluding outer .040")
	2.000" Diameter -	0.002" max. (excluding outer .040")
	3.000" Diameter -	0.003" max. (excluding outer .040")
Flat Width	1.500" Diameter -	0.625" ±0.125"
	2.000" Diameter -	0.625" ±0.125"
	3.000" Diameter -	0.875" ±0.125"
Diameter	±.010"	
Edge Chips	Not to exceed 10 chips per substrate. Chips shall be less than 0.125" deep and less than 0.375" long. 90% of the substrates to have no chips > 0.040" deep.	
Parallelism	.001"/Inch of Diameter	
Backside	≤32 Microinches, CLA	

*SOS-10
May 15, 1974
Rev. A - 2/14/75

Table 2-2. (Continued)

Silicon Epitaxial Film:

A.	Type	-	As Specified
B.	Concentration	-	As Specified
C.	Thickness	-	As Specified
D.	Surface Finish		

The following describes a consistent method to evaluate epitaxial silicon films on sapphire substrates. A microscope is not used, only artificial light most suited to the particular defect definition is used.

1. Procedure:

Under a bright light (preferably a flood lamp), the substrate is rotated until it is approximately 45 degrees to the light beam. The entire surface is scanned and the results from the back reflections are noted. This method is best suited to scratch definition and pit definition.

2. Epitaxial Film Evaluation:

a.	Pits	-	Under the bright light test, there shall be no more than 4 pits per substrate. The pits shall not be larger than 50 microns.
b.	Scratches	-	Under the bright light test, there shall be no scratches greater than 0.5 inches long and the combined length of all scratches shall be less than 2.0 inches. Ninety (90) wafers out of a lot of one hundred (100) wafers will have no scratches.
c.	Haze	-	Under fluorescent light there shall be no haze visible on the epitaxial film.
d.	Resistivity and Film Thickness	-	Both shall be measured in the center of the wafer.
e.	Spikes	-	No visible spikes greater than one times film thickness are acceptable.
f.	Orange Peel	-	None
g.	Dislocation Density	-	None visible at 100X after light Sirtl etch.

Table 2-2. (Continued)

E. Lot Size	-	100 wafers or less
F. Certification	-	A certificate of compliance to these specifications will be issued with each lot.
G. Packaging	-	a. Wafers will be packaged in a manner such that they will be free from wax, dirt, grease, or other surface contamination after a standard solvent cleaning. b. Wafer containers will be clearly labeled showing type, concentration, diameter, thickness, lot number and purchase order number.

2.5 Wafer Inspection - Lot 610

Prior to the start of processing, the wafers were inspected using the techniques outlined in Appendix A.

A visual scan of the wafers using a Nomarski interference contrast filter revealed scratches on the sapphire on wafers 9, 10 and 11 only. These scratches, which resulted from a planned reduction in polishing time are easily distinguished from the small scratches caused by handling damage which occur in the silicon at the outer wafer edges. The scratches, similar in all three wafers, ranged in length from 0.13 cm to 2.0 cm and from 0.1 μm to 0.2 μm in width. No attempt was made to measure the depth of the scratches.

The surface texture of the film, excluding scratches, was noted to have a slight increase in graininess (roughness) going from the select finish, to the standard finish, to the inferior finish.

The results of IR spectrophotometer measurements and sodium light topographs, as shown in Table 2-3, showed silicon film thickness variations ranging from 1000 Å to 2000 Å. The films were generally found to be thinner at one edge of the wafer and to increase in thickness in a monotonic manner toward the opposite edge. There was no indication of a "ripple effect" of alternately thinner and thicker silicon. The average film thickness on wafers in lot 610 was 7260 Å.

Table 2-3. Wafer Inspection Prior to Device Fabrication

Wafer No.	Polish Quality	No. of Fringes	Minimum Thickness, μm	Maximum Thickness, μm
610.1	Standard	1.9	0.68	0.83
610.2	"	2.1	0.61	0.78
610.3	"	2.3	0.63	0.81
610.4	"	2.5	0.60	0.80
610.5	Select	1.7	0.70	0.83
610.6	"	1.3	0.67	0.77
610.7	"	1.8	0.61	0.75
610.8	"	-	0.72	0.85
610.9	Inferior--75%	2.3	0.64	0.82
610.10	" --75%	1.9	0.63	0.78
610.11	" --75%	2.0	0.64	0.80
610.12	" --50%	2.3	0.65	0.83

2.6 Device Fabrication - Lot 610

Four wafers from each polishing variation (standard, select and inferior) were processed in one 12-wafer lot, designated lot 610. CMOS inverter circuits (4007SR) were fabricated on these wafers according to the process outlined in Appendix B. Four wafers (610.4, 610.5, 610.8, and 610.11) were broken during fabrication. These broken wafers could not be probed for the yield analysis experiment, and consequently, no characterization was done on them.

Wafers 610.9 and 610.10, which had a 75% reduction in final polish time, had marks in the silicon apparently corresponding to scratches in the sapphire. These marks were still apparent after device fabrication.

2.7 Wafer Probe Results - Lot 610

The wafers were probed and the resulting data were mapped and sorted. Yields were calculated as described in Appendix C. The four broken wafers (610.4, 610.5, 610.8 and 610.11) could not be probed on the automatic probe. The wafer maps did not show effects corresponding to either the thickness variation across the wafer or to the scratches on 610.9 and 610.10. The wafer maps in general did not show local variations--the failures appeared randomly distributed over each wafer.

The yield results for lot 601 wafers are presented in Table 2-4. In the failed dice column, it is apparent that there is little difference between the standard and select polish, but that the inferior polish gives a significant improvement in yield. Closer inspection of these results reveals that the die yield on the wafer having a 50% reduction in final polish time (610.12) is

Table 2-4. Yield Results From Lot 610--Sapphire Polish Variation

Numbers shown are numbers of failures. Note that there are 300 dice with 900 inverters (900 p-channel and 900 n-channel transistors per wafer).

SAPPHIRE POLISH	WAFER NUMBER	FAILED DICE	FAILED INVERTERS	p-CHANNEL	n-CHANNEL	p-CH LEAKAGE	n-CH LEAKAGE	p-CH VOLTAGE	n-CH VOLTAGE	p-CH GATE LEAKAGE	n-CH GATE LEAKAGE
Standard	610.1	202	319	129	271	81	253	1	6	48	15
Standard	610.2	178	273	165	209	149	197	3	4	15	12
Standard	610.3	281	588	321	492	247	438	19	24	70	49
	AVERAGE										
	%	73	44	23	36	17	33	0.8	1.3	4.9	2.8
Select	610.6	181	291	139	239	115	226	0	3	24	13
Select	610.7	243	446	202	371	150	339	3	11	49	25
	AVERAGE										
	%	71	41	19	34	15	31	0.2	0.8	4.1	2.1
Inferior	610.9	111	158	107	93	86	60	2	7	19	39
Inferior	610.10	147	218	104	165	83	147	3	8	18	12
Inferior	610.12	281	587	351	474	299	418	2	3	52	55
	AVERAGE										
	%	60	36	21	27	17	23	0.3	0.7	3.3	3.9

NOTE: Failure criteria are; channel leakage $>10^{-7}$ amps at V_{DS} = 10V, voltage drop > 0.5V at 3 ma load, and gate leakage $>10^{-6}$ amps at $V_G = \pm 10V$

quite similar to wafers from the standard or select groups, but that the two wafers having the 75% reduction in final polish time (610.9 and 610.10), and having visible scratch marks, show a much improved yield. This leads to the rather surprising conclusion that the final polishing step, which removes visible scratches from the sapphire surface, might be actually detrimental to the quality of silicon grown on the sapphire. Further inspection of Table 2-4 reveals that the n-channel failure rate is significantly higher than the p-channel failure rate and that the superior yield in wafers 610.9 and 610.10 is associated only with the n-channel transistors. Finally, it is apparent that almost all of the failures in both n-channel and p-channel transistors are leakage current failures and that wafers 610.9 and 610.10 exhibit many fewer n-channel leakage current failures than other wafers in this lot. It must be remembered, however, that the channel leakage is the first measurement tested and that transistors failing this test are not tested for voltage drop or gate leakage.

The results of sorting the various measurements are shown in the distribution curves of Figures 2-1 through 2-4. It is characteristic of this lot that the leakage currents either fall within the rather narrow distributions shown in Figure 2-1 or they are beyond full scale of the measuring instrument (200 nA). The gate leakages are essentially all either less than 200 nA or greater than 2 μA and are not plotted. The height of the various distributions is related to the number of devices tested, which is different for the three different polish variations and may vary also with the type of measurement and from wafer to wafer, due to the order and hierarchy of testing, as described in Appendix C. There appears to be little difference between the p-channel distributions for the different polish variations, or in the median of the various distributions for the n-channel transistors. However, the n-channel leakage distribution for the inferior polish group is slightly broader than for the other two variations, while the n-channel voltage drop distribution is broader for the select polish, and both the standard and select polishes show a broader n-channel threshold voltage distribution than the inferior polish. No major significance is attributed to these differences, as they are not great enough to impact device performance.

Measurements of field-effect mobility were taken at several locations on each wafer in an independent probing operation, as described in Section C-4 of Appendix C. These measurements were made on the test structures located between 4007SR dice on alternate rows of the wafer. The results are shown in Table 2-5. There is no significant dependence of field-effect mobility on sapphire polish quality.

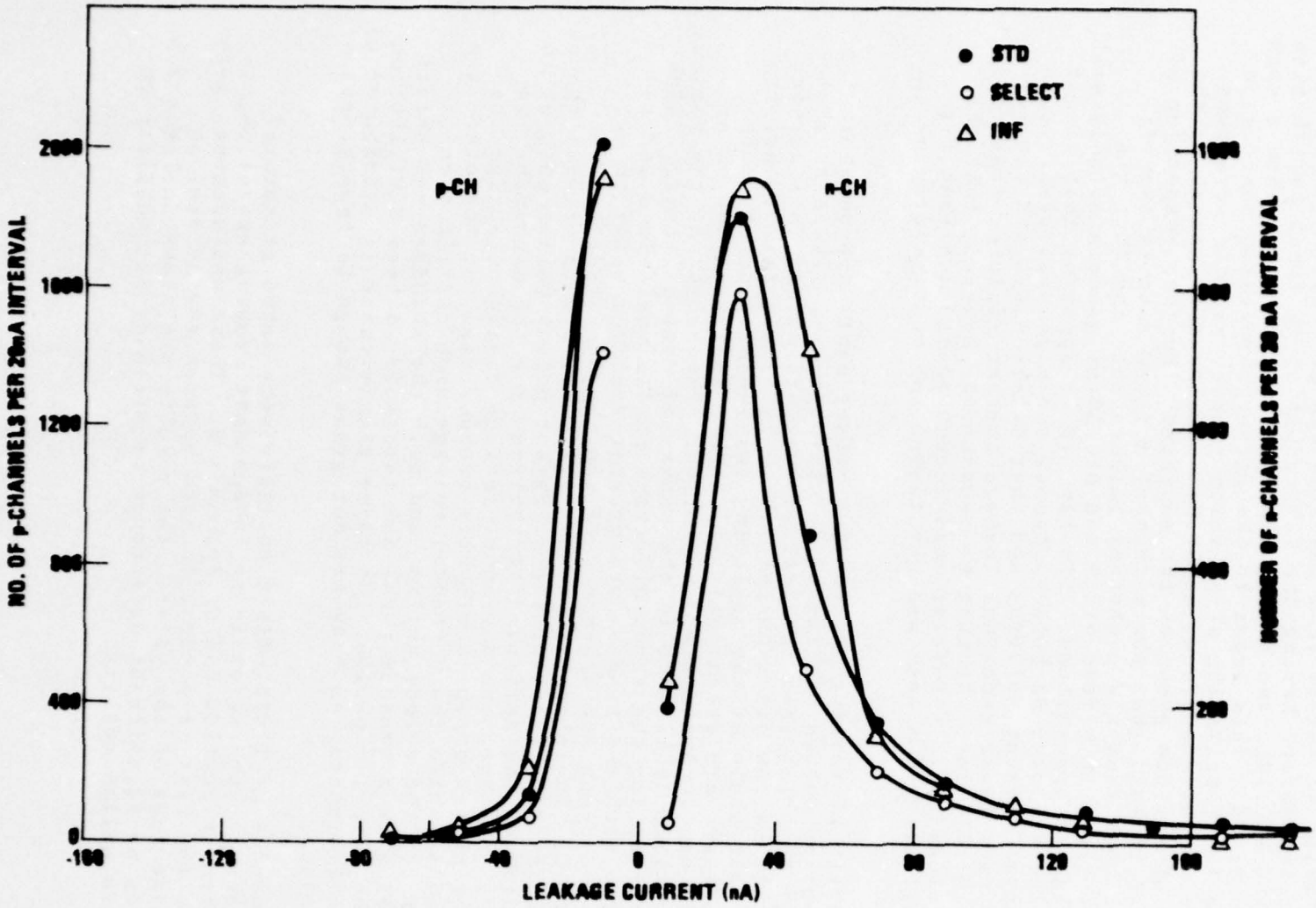

Figure 2-1. Effect of Sapphire Polish on Drain Leakage

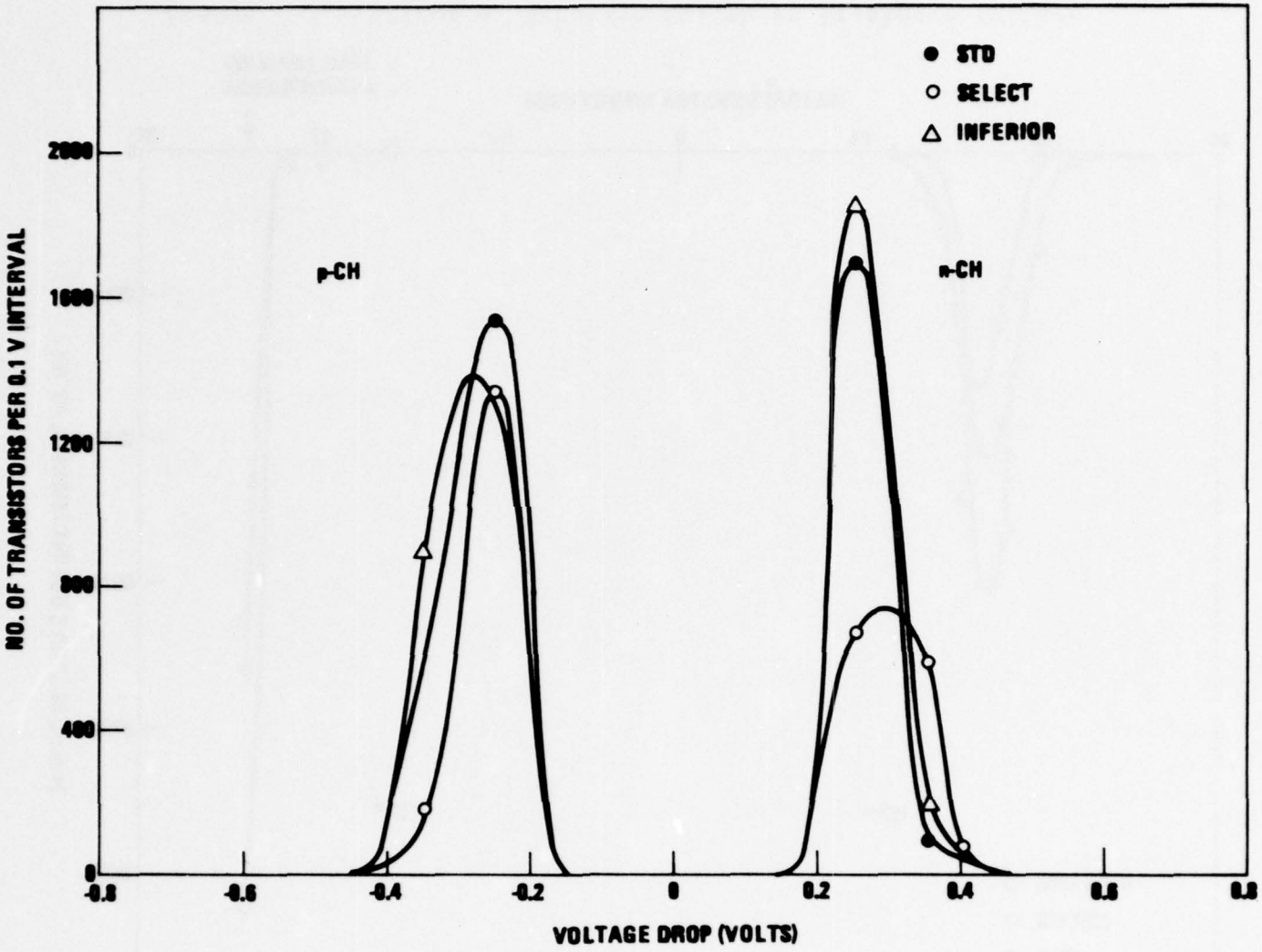

Figure 2-2. Effect of Sapphire Polish on Voltage Drop

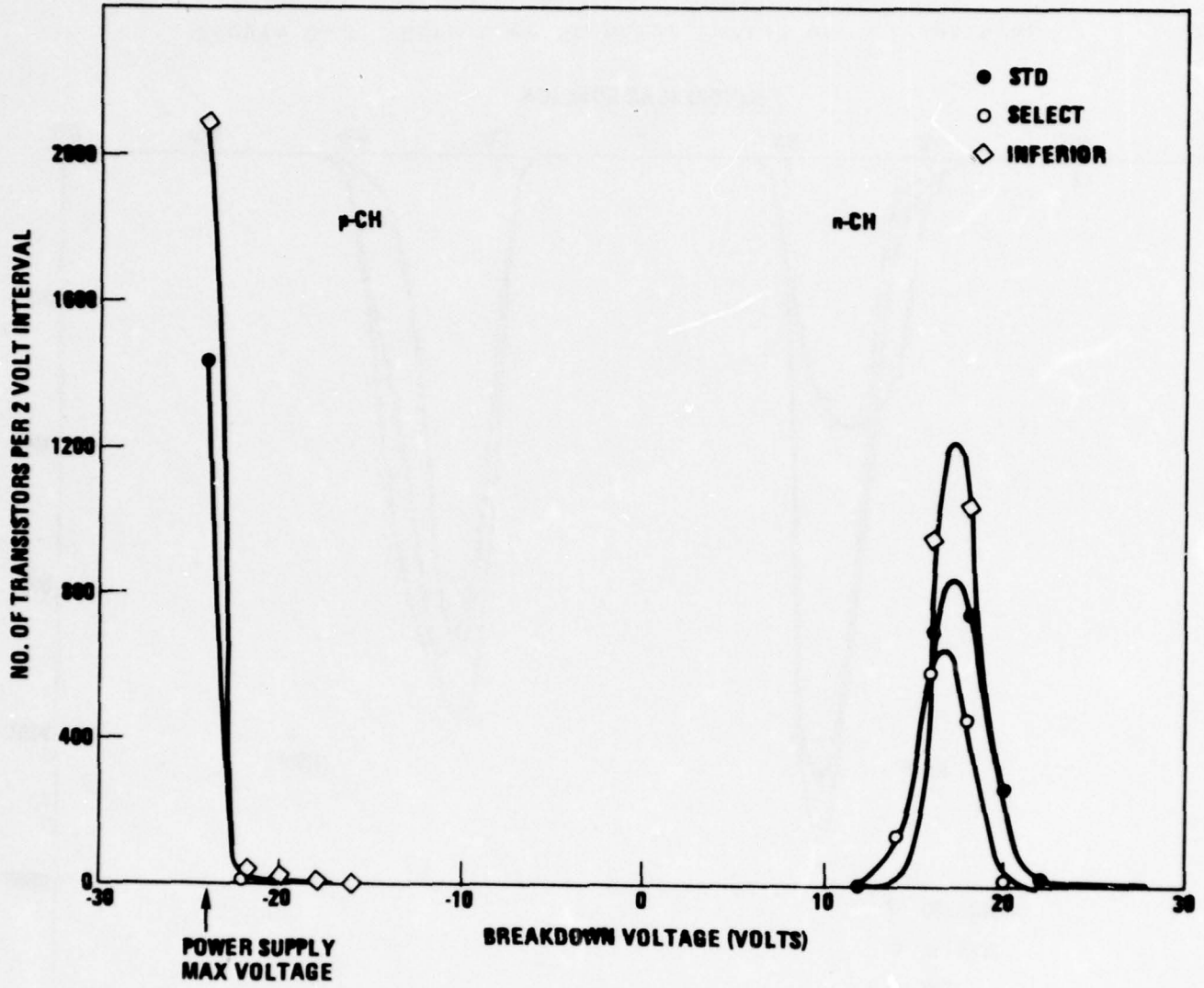

Figure 2-3. Effect of Sapphire Polish on Breakdown Voltage

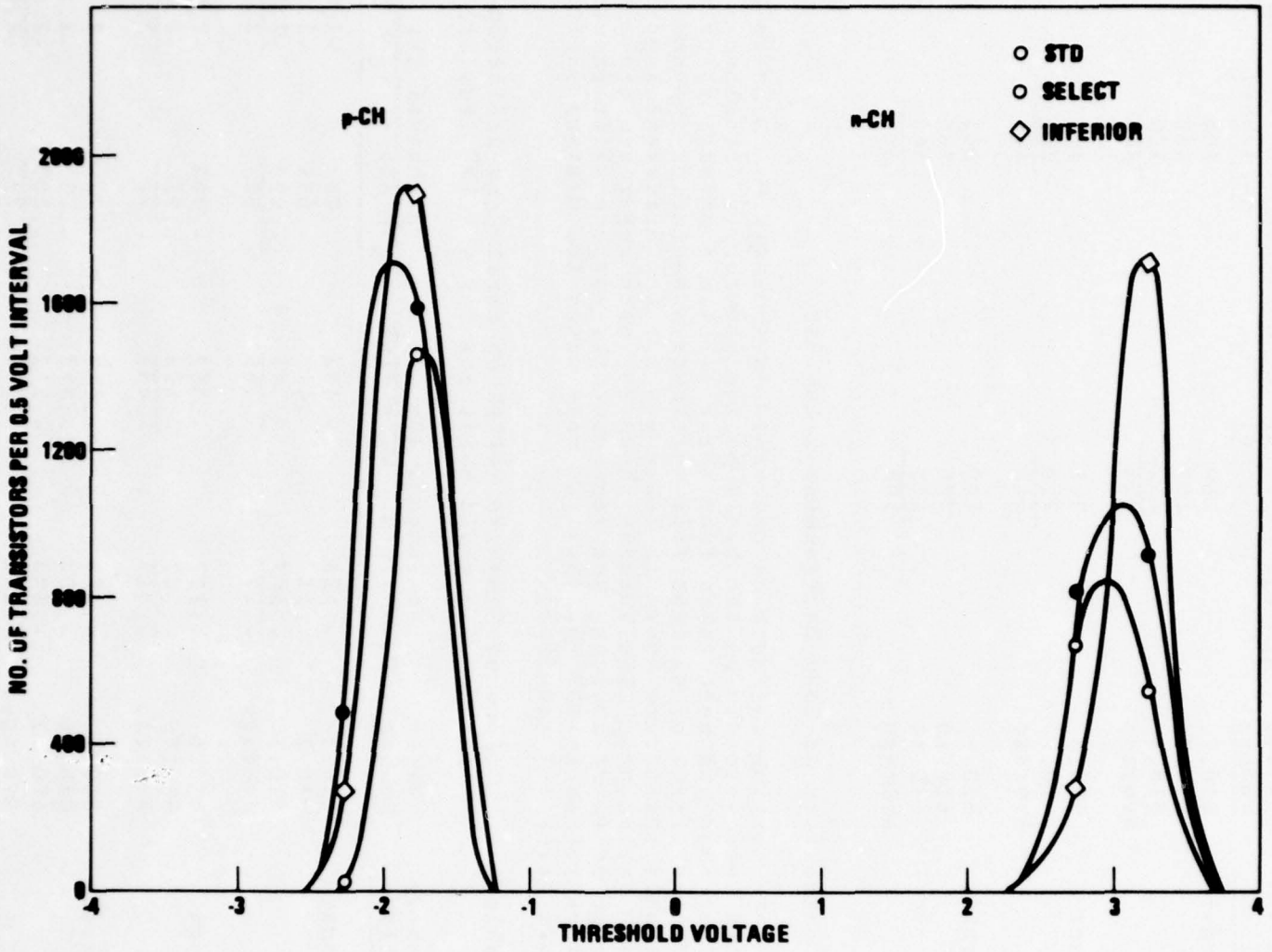

Figure 2-4. Effect of Sapphire Polish on Threshold Voltage

Table 2-5. Effect of Sapphire Polish on Field-Effect Mobility

Sapphire Polish	Wafer Number	Average Field-Effect Mobility ($cm^2\ V^{-1}\ sec^{-1}$) p-channel	n-channel
Standard	610.1	209	354
	610.2	209	365
	610.3	252	329
	Average	223	349
Select	610.6	213	403
	610.7	210	393
	Average	212	398
Inferior	610.9	190	363
	610.10	226	360
	610.12	179	363
	Average	198	362

2.8 Stability in Co^{60} Environment - Lot 610

The Co^{60} testing was done as described in Appendix D. Dice to be tested were selected on the basis of the previously described failure maps and were taken from three locations on each wafer to study the effect of silicon film thickness. Radiation-induced threshold shifts are shown in Table 2-6 for the different sapphire polish variations. The numbers shown for each wafer are the average of three devices, and represent the maximum shift induced by irradiation to 10^6 rads(Si) [in some cases the maximum shift occurs below 10^6 rads(Si)].

Table 2-6. Effect of Sapphire Polish on Worst-Case Radiation-Induced Threshold Shift for $0 < \gamma < 10^6$ rads(Si)

Sapphire Polish	Wafer Number	n-channel ΔV_T $V_G = -10$ V	$V_G = +10$V	p-channel ΔV_T $V_G = -10$V	$V_G = +10$V
Standard	610.1	-.123	-.453	-.71	-2.44
	610.2	-.12	-.41	-.685	-2.5
	610.3	-.567	-.593	-1.093	-2.59
	Average	-.27	-.485	-.83	-2.51
Select	610.6	-.127	-.353	-.603	-2.21
	610.7	-.507	-.523	-.92	-2.25
	Average	-.317	-.438	-.76	-2.23
Inferior	610.9	-.153	-.487	-.71	-2.49
	610.10	-.107	-.417	-.72	-2.56
	610.12	-.403	-.513	-.883	-2.43
	Average	-.221	-.472	-.77	-2.49

There is little difference between the average radiation-induced threshold shift at a given bias condition for the different qualities of sapphire polish. The wafer-to-wafer variation, however, is relatively large, except in the case of the p-channel, positive bias case. This case produces the largest radiation-induced threshold shifts and does indicate a slight improvement in radiation hardness for the select polish. This improvement is not large enough to be significant from the standpoint of circuit performance.

Radiation induced n-channel leakage currents are shown in Table 2-7. No p-channel leakage increase was observed. The maximum n-channel leakage often occurred at doses below 1 megarad, in which case the maximum leakage current measured is tabulated for three devices on each wafer along with the corresponding radiation dose. Also shown is the starting thickness of the silicon film at the location on the wafer from which the device was taken. The radiation bias condition for maximum n-channel leakage was V_{DD} = +10 V and V_{GS} = 0, while the measurement bias is V_{DD} = +10 V and V_{GS} = - 10 V. The results indicate little difference between the standard and select sapphire polishes but that the inferior polish gives a very definite reduction (about a factor of two) in radiation induced leakage. A rather striking feature of the results is the correlation between radiation induced leakage and silicon film thickness. The maximum radiation induced leakage current is seen to be a strongly decreasing function of silicon film thickness. This is shown in Figure 2-5 where maximum radiation-induced leakage is plotted against starting silicon film thickness.

There was no significant change in gate leakage induced by any of the radiation tests.

2.9. Stability Under Bias-Temperature Stress - Lot 610

Bias-temperature measurements were done on one or two dice from each wafer as described in Appendix E. Initially the devices were stressed at the three different bias conditions for 16 hours at 200°C. However, the changes produced by this test were hardly measurable, so the same devices were stressed again for 16 hours at 260°C. Changes were still very small. Under the two static bias conditions, leakage currents remained less than 1 μA, threshold shifts remained less than 0.3 V, and transconductance changes were less than 15%, except in two cases. These two cases were wafers 610.2 and 610.10. On wafer 610.2, devices on both dice tested exhibited n-channel leakages of ~5 μA for the positive drain bias case, while the devices on one die showed threshold shifts in excess of 0.6 volt for both static bias conditions and a 40% decrease in n-channel transconductance. In the case of wafer 610.10, p-channel threshold shifts were about 0.6 V for both static bias conditions, while the n-channel leakage current was 1.8 μA in the positive drain bias case, and n-channel transconductance decreased by about 30%. Changes in gate leakage

Table 2-7. Effect of Sapphire Polish on Radiation-Induced n-Channel Leakage

Polish	Wafer	Device	Leakage(μA)	Dose(rads)	Si Thickness(μm)
Standard	610.1	1606	80.69	10^5	0.69
		1616	48.2	10^6	0.78
		1628	24.4	10^6	0.83
	610.2	2706	257	10^6	0.61
		1516	234	3×10^5	0.71
	610.3	2020	87.7	10^6	0.76
		2920	143	10^6	0.68
		0908	21	10^6	0.83
	Average		110		
Select	610.6	2206	177	3×10^5	0.76
		2216	117	10^6	0.77
		2228	114	10^6	0.74
	610.7	0420	246	3×10^5	0.64
		1620	120	3×10^5	0.76
		2720	63	3×10^5	0.8
	Average		123		
Inferior	610.9	0712	8	3×10^5	0.8
		1812	45	10^6	0.74
		2612	75	10^6	0.7
	610.10	0718	141	10^6	0.68
		1918	83	10^6	0.72
		2618	54	10^6	0.75
	610.12	0916	7	10^6	0.82
		2316	16	10^6	0.75
		2818	49	10^6	0.71
	Average		53		

Notes: 1. Radiation doses tabulated above are doses for which the maximum leakage current was measured in the range from zero to 10^6 rads(Si).

2. Devices were 40 mil wide n-channel transistors on CMOS/SOS 4007SR devices.

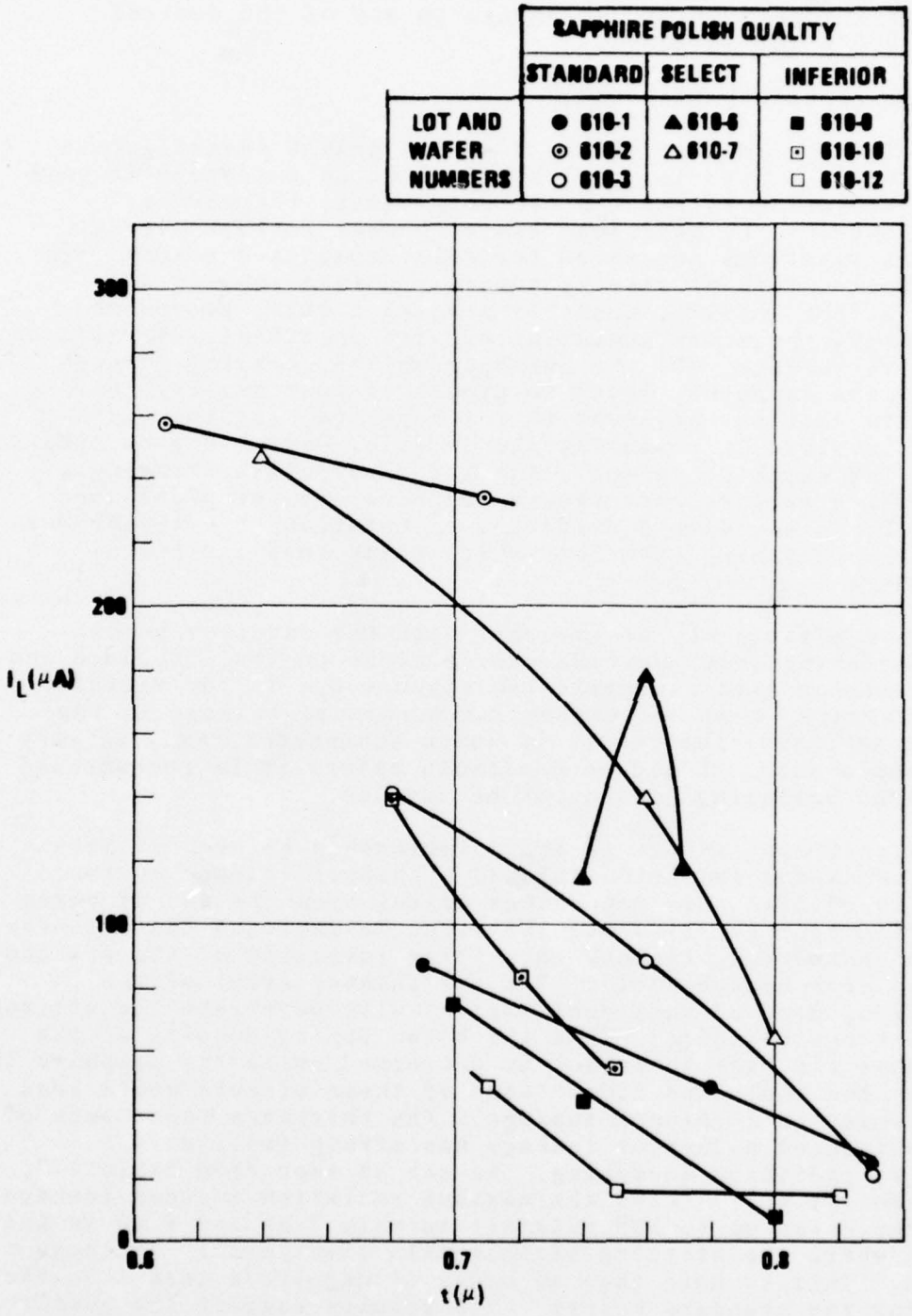

Figure 2-5. Maximum Radiation-Induced Leakage vs. Silicon Thickness for Sapphire Polish Variations

during the bias-temperature tests were negligible. Under dynamic bias, there was no significant change in any of the devices tested at 260°C for 16 hours.

2.10 Sapphire Polish Results

The most striking feature of the sapphire polish investigation has been that the inferior polish has shown an advantage in both yield and radiation tolerance. In both cases, the device parameter showing the advantage was n-channel leakage current. Possible explanations suggested for this unexpected result are (1) the final polishing step is actually deleterious to the sapphire surface quality, possibly leaving a thin, amorphous layer of Al_2O_3, possibly contaminated with polishing materials on the sapphire surface, (2) the inferior polish, leaving a rough surface on the sapphire, leads to growth of poor quality, very low mobility, silicon adjacent to the sapphire, (3) the extra polishing involved in producing the inferior polish may be beneficial to the sapphire, and (4) the inferior polish, leaving a rough sapphire surface, may expose sapphire crystal planes upon which silicon grows with a different orientation, thereby producing a silicon/sapphire interface which traps less radiation-induced charge.

All of these effects may be present, with the inferior polish sapphire trapping less positive charge close to the interface and yielding silicon with extremely low conductance in the vicinity of the interface, thus decreasing the n-channel leakage in two ways. In any case, the result is quite unexpected, and, in view of the sample size, should be confirmed before it is recommended that present polishing procedures be revised.

Another significant result is the relationship between silicon film thickness and radiation induced n-channel leakage current. It is believed that this dependence arises from the use of boron implantation near the $Si-Al_2O_3$ interface to increase the acceptor doping concentration, thereby inhibiting inversion of the silicon (formation of a backchannel). For the thinner areas of the silicon film, most of this deep implant will penetrate the silicon and stop in the sapphire. Thus the boron doping density of the silicon near the back interface is decreased, while the sapphire is damaged by the implanted ions. Both of these effects would lead to an increase in n-channel leakage. The thickness dependence of radiation-induced n-channel leakage has strong implications relative to radiation hardening. As can be seen from Table 2-7, in the inferior polish case the maximum radiation induced leakage current for doses up to 10^6 rads(Si) is only 7 μA and 8 μA in the two cases where the starting silicon film thickness is as large as 0.8 μm. This is more than an order of magnitude less than the average for the standard wafers. The results suggest the possibility of achieving very low radiation-induced leakage on a regular basis, either through much better control of the silicon film thickness or through an improved ion implantation method or some combination of both.

Other than the leakage current effects, no significant differences were found between the various sapphire polish qualities. In probing for yield, neither the p-channel parameters nor the n-channel voltage drop (related to mobility values) and gate leakage showed any significant dependence on quality of sapphire polish. The average field-effect mobility for the different cases was also independent of sapphire polish. Likewise, the radiation-induced threshold shift and the bias temperature results show no dependence on sapphire polish. Thus we have the surprising conclusion that a significant improvement in n-channel leakage, both from the yield standpoint and from the radiation hardness standpoint can be achieved by reducing the final polish time, while no other advantages or disadvantages are apparent for any of the three qualities of sapphire polish investigated.

Finally, it is appropriate to recommend additional experimental confirmation, based upon the small sample size (8 wafers) from which these conclusions have been made.

3. SAPPHIRE CLEANING EXPERIMENTS

The IMMA work on Phase I of this contract showed a strong correlation between device yield and quality and the presence of impurities in the silicon. One very important source of impurities in the silicon is the sapphire surface upon which the silicon is grown. Due to the thinness of the silicon layer (0.75 μm), comparatively small surface concentrations of impurities on the sapphire can result in significant impurity concentrations in the very small volume of silicon. Thus it is important to identify cleaning procedures leading to either very clean sapphire surfaces or at least sapphire surfaces having a minimum of detrimental impurities. It should be noted that certain cleaning procedures, designed to remove one type of impurity, might themselves introduce another, more harmful impurity. The experiments described in this section were designed to investigate the effect of three variations in sapphire cleaning procedures on the quality of SOS material as determined by the yield, electrical characteristics and stability in radiation and high-temperature environments.

3.1 Material Fabrication

3.1.1 Background to Cleaning Approaches

Recent processing results at several SOS device manufacturers have indicated that substrate cleaning, particularly the pre-epitaxy cleaning process, is critical to device performance and yields. Polishing compound residues, mobile ion contaminants, organic solvent residues, and statically-held particulates on the substrate surface are thought to be the causes of high leakage currents in n-channel transistors, wafer-to-wafer variations, low CMOS/SOS device yields, and unstable resistivity values. Many changes were made in the cleaning procedure over the past two years in order to minimize each contaminant as it was reported by device manufacturers. Rigorous, detailed substrate cleaning prior to epitaxy has resulted in recent user reports of high yields, improved device parameters, lot-to-lot consistency, and successful LSI circuit fabrication.

Historically, the basic pre-epi cleaning procedure for sapphire substrates used until recently was designed and used as part of the fabrication process in 1971. The increased demand for SOS wafers justified the establishment of a separate cleaning facility at UCC in 1971. The basic procedure is listed in Table 3-1. The final pre-epitaxial cleaning step consisted of a hand-scrubbing of the substrate surface, using an acetone-loaded Kimwipe. Each substrate was manually wiped, being held in a vacuum chuck and illuminated with a microscope lamp. A filtered nitrogen blow gun was then used to remove any loose particulates as the substrates were loaded into the reactor.

Table 3-1. Cleaning Procedure 1971 - July 1975

Manufacturing Sequence

Finished Substrate

↓ (clean)*

Clean Substrate

↓ (inspect)

Accepted Substrate

↓ (package)

Substrate Inventory

↓ (Pre-epitaxial clean)**

Epitaxial Preparation

↓ (Film deposition)

Epitaxial Wafer

↓ (Inspect)

Accepted Wafer

↓ (package)

Wafer Inventory

***Cleaning Procedure**

I. Gross Contaminant Removal
   - A. Ultrasonic agitation of detergent solution at 80°C for 15 min.
   - B. D.I. water rinse for 15 min.

II. Chemical cleaning
   - A. Aqua regia acid boil for 15 min
   - B. D.I. water rinse for 15 min
   - C. Sulfuric acid at 80°C for 15 min
   - D. D.I. water rinse for 15 min

III. Drying
   - A. D.I. water rinse for 15 min
   - B. Spin dry in warm, dry nitrogen atmosphere

****Pre-epitaxy Cleaning Procedure**

I. Manual Substrate Scrub
   - A. Secure substrate onto vacuum chuck
   - B. Wipe surface with acetone-loaded Kim-Wipe leaving clean surface with no smears
   - C. Blow surface with dry, filtered nitrogen
   - D. Load onto susceptor

This procedure seemed to work well for some time (1971 - 1975), and device manufacturers had no adverse comments on surface cleanliness quality or related device performance. A history of device processing experience, larger scale SOS device development programs at more companies, related bulk silicon processing experience, and the move to the more complex LSI circuitry demanded materials improvements, beginning in early 1975.

The first request for improved quality involved the particulate contaminants on the substrate surface that subsequently interfered with CMOS/SOS device yields, particularly in LSI device. These particulates were statically attracted and thus held tightly to the substrate surface. The final pre-epitaxial cleaning did not remove these particulates efficiently or consistently, and subsequent film deposition would cause projections or spikes in the film. These defects would scratch the photomasks and lower yields by interfering with line geometry and initiating further defects in subsequent processing. These particulates appeared to be common dust particles present in the ambient atmosphere, cleaning tanks, and rinse water supply. A concentrated effort began in early 1975 to improve the cleaning procedure in order to minimize or eliminate these particulates.

Particulates were reduced by installing sub-micron size filters on water lines and nitrogen lines, and installing an automatic wafer scrubber to be used for the final cleaning just prior to film deposition. The wafer scrubber, illustrated in Figure 3-1, is Model C-2WS, made by II Industries, Sunnyvale, California. The manufacturer recommended that a cleaning cycle of detergent-brush scrub, ammonia rinse, isopropanol rinse, and spin dry be used. This procedure was followed and particulate contamination was greatly reduced. The automatic scrubber was used as part of the manufacturing process in July 1975. User reports on SOS devices made with scrubbed substrates were quite encouraging, indicating the particulate counts were greatly reduced, yields improved, and device performance improved. At Rockwell International, comparison of two lots, reflecting SOS wafers made prior to and after scrubber installation, gave significantly different leakage currents as reported in Reference 1. Rockwell CMOS/SOS Lot A had higher leakage current values, and wafers from this lot were fabricated prior to the scrubber installation at UCC. Rockwell CMOS/SOS Lot B had lower leakage current values and was made after the scrubber installation. Other users reported improved yields and successful fabrication of devices at the LSI complexity level. Table 3-2 lists the pre-epitaxial procedure used at that time.

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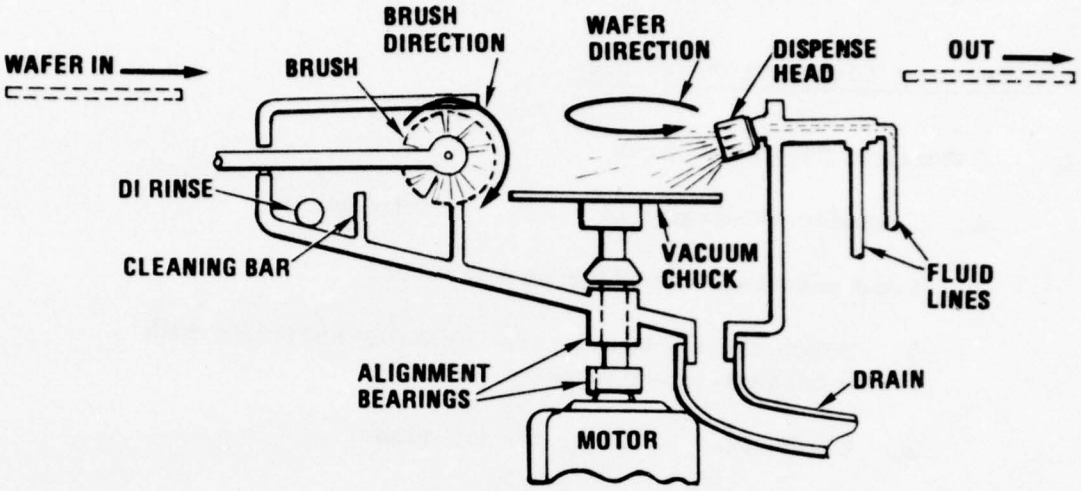
1. RADC-TR-76-208, Interim Technical Report, "Investigation of Defects and Impurities in Silicon-on-Sapphire," July 1976



I. Load Cycle
   A. Substrate is brought from cartridge to position on vacuum chuck

II. Scrub Cycle
   A. Vacuum chuck lowers into scrubbing position
   B. Substrate is spun at selected speed while held in place by vacuum chuck. Spindle range is 0–10,000 RPM.
   C. Revolving roller-type brush contacts spinning substrate.
   D. Liquid detergent is applied to substrate and scrubbing action continues for present time. Time range is 0–99 seconds.

III. First Rinse Cycle
   A. Brush contact may be maintained if desired.
   B. Rinse solution is applied to spinning substrate and continues for preset time.

IV. Second Rinse Cycle
   A. Rinse solution is applied to spinning substrate and continues for preset time.

V. Dry Cycle
   A. High speed spin of substrate is continued for preset time.
   B. Dry, filtered, anti-static nitrogen is blown onto substrate to promote drying action.

Figure 3-1. Automatic Wafer Scrubber

Table 3-2. Changes in Pre-Epitaxial Cleaning Procedure-July 1975

Pre-Epitaxy Cleaning Procedure

I. Automatic Substrate Scrub

A. Transfer substrates to scrubber cartridge

B. Load substrate cartridge into scrubber

1. Scrub cycle - brush scrub spinning substrate with detergent-water mixture

2. First rinse - dilute NH_4OH rinse

3. Second rinse - Isopropanol rinse

4. Dry - High speed spin with blowing dry nitrogen

C. Unload substrate cartridge with cleaned substrates and store in Laminar Flow Hood.

D. Load substrates onto susceptor, using dry, filtered, anti-static nitrogen to blow off surface.

The second area of surface cleanliness improvement was the more efficient removal of polishing compound residues and loose Al_2O_3 particles from the grinding operation. In-house yields in the UCC Epitaxial Department showed that polishing compound removal was not being accomplished efficiently or consistently. Changes in the basic procedure occurred from September through November 1975. Some of the solutions investigated efficiently removed polishing compound residues, but contained sodium, These solutions were replaced since users were quite concerned about mobile ion contaminants remaining on the surface and effecting device properties. By November 1975, all solutions known to contain mobile ions as a majority constituent were eliminated from the cleaning procedure. Table 3-3 lists the cleaning procedure as it existed in September 1975 and the current procedure as instituted in November 1975.

Table 3-3. Changes in Substrate Cleaning Procedure-
September - November 1975

Cleaning Procedure

September 1975	November 1975
I. Polishing Residue Removal	I. Polishing Residue Removal
A. Experimental acids, bases, solvents	A. Detergent solution
II. Gross Contaminant Removal	B. Rinse and dry
A. Ultra-sonic agitation of detergent solution at 80°C for 15 min.	C. Hot solvent
B. D.I. water rinse for 15 min.	D. Dry
III. Chemical Cleaning	E. Ultrasonic agitation of detergent solution at 80°C
A. Aqua regia acid boil for 15 min.	F. D.I. water rinse
B. D.I. water rinse for 15 min.	II. Chemical Cleaning
C. Sulfuric acid at 80°C for 15 min.	A. Reducing acid - oxidizing acid
D. D.I. water rinse for 15 min.	B. D.I. water rinse
IV. Drying	C. Dry
A. D.I. water rinse for 15 min.	D. Ultrasonic agitation of hot solvent
B. Spin dry in warm, dry nitrogen atmosphere	
V. Pre-Epitaxial Clean	E. Dry
A. See Table 3-2.	1. See Table 3-4.

Polishing compound residues are not always visible prior to epi, and thus may avoid detection until a film is deposited. After epi, these residues appear as boat marks or smears, generally near the wafer edge. These marks or smears have a gray, cloudy appearance and the pattern suggests that the cleaning process was inefficient. It was thought that these residues may be the source of the impurities noted in Reference 1. It was postulated that these impurities could be present as a result of inefficient polishing compound removal, and may be present even though the tell-tale marks and smears are removed. Loose Al_2O_3 particles on the surface from the sapphire fabrication process may be the source of Al found in the surface analysis. By November 1975, a process was established that is believed to be efficient and consistent in removing polishing compound residues and Al_2O_3 particles.

The third area of surface cleanliness improvement was made in cooperation with a major user, and concentrated on surface residues left from the scrubber cycle, just prior to epi. This user reported wide lot-to-lot and wafer-to-wafer variations in n-channel leakage currents, with wafers delivered prior to July 1975 much better than post-July 1975 deliveries. Average leakage values were less than 10 nA/mil for the older lots, while post-July lots varied from 10 to 300 nA/mil, with most of the wafers in the lots having leakage values approaching 100 nA/mil. Associated with the problem of high leakage currents was a problem of unstable resistivity values. The intrinsic resistivity value of the film would be measured immediately after deposition, and a high value, >300 ohm-cm, type indeterminate, recorded. After shipment, the original value could not be remeasured on many of the wafers. In some cases, the original value could be reproduced, but only after several measurements. Returned wafers were remeasured, and original values were observed, although sporadically.

The high leakage current and unstable resistivity problem seemed to occur after installation of the wafer scrubber. Surfaces were much cleaner visually, having very few particulates, but were postulated to have cleaning solvent residues that affected electrical properties. The recommended final isopropanol rinse in the wafer scrubber, Table 3-2, was postulated to be the source of these residues. At this point in time, reports from bulk silicon users indicated that bulk device yield and electrical parameters were being affected by the use of organic solvents in the automatic wafer scrubber cycles. Efforts were begun in November 1975 to eliminate these residues, and still produce particle-free films. The wafer scrubber was retained as part of the process, since this was necessary for particulate removal.

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1. RADC-TR-76-208, Interim Technical Report, "Investigation of Defects and Impurities in Silicon-on-Sapphire," July 1976

The scrubber cycle was modified so that the organic solvent rinse as shown in Table 3-4 was eliminated. Another final cleaning process was designed using the isopropanol rinse cycle in the scrubber, but adding a boiling oxidizing acid step, followed by a deionized water rinse. This is shown in Table 3-4, alternate procedure. These tests were conducted in November - December 1975, and the user reported greatly improved properties of devices made with the acid-washed wafers. The user reports that all wafers supplied since December 1975 have had very low leakage values, from 1 to 5 nA/mil, with most of the wafers at <2 nA/mil. All of these substrates had been acid washed to oxidize organic solvent residues on the surface. For substrates that had been cleaned using a final water rinse in the scrubber, eliminating the organic solvent, somewhat higher leakage values were attained, from 17 - 30 nA/mil. The user also reported that as-received resistivity values had stabilized. This was confirmed as originally-measured values were reproducible, and values were stable over long periods of time.

Since December 1975, no organic solvents have been used in the final cleaning steps. Since this time, other users have reported higher device yields, lower carrier concentrations (higher resistivity) for intrinsic films, stable resistivity values remaining high after high-temperature oxidation, and lower leakage current values.

3.1.2 Sapphire Cleaning Variations

At the start of this program (January 1975), cleanliness of the pre-epitaxial surface was thought to be of critical importance to device parameters. Subsequent evaluations by other users tend to confirm this view. Experimental lots 7 - 9 were designed to study the pre-epitaxial cleaning variations. Experimental Sets III and IV were designed to provide additional cleaning action or modification of the silicon-sapphire interface.

Three variations on the standard sapphire cleaning procedure were examined. The standard procedure uses an acid wash followed by a rinse and a scrub cycle. No alcohol is used in the rinse or scrubber cycles. The first variation on this procedure uses isopropyl alcohol as a final rinse in the scrubber cycle. The second variation was to first clean the sapphire using isopropyl alcohol in the scrubber cycle and to follow this with an acid wash and a rinse. The third variation was to eliminate all detergents and organics from the scrubber cycle in the otherwise standard cleaning procedure. Thus, experimental lot number 7 reproduced the pre-epitaxial cleaning process used from July - November 1975, as listed in Table 3-2. Experimental lot number 8 reproduced the pre-epitaxial cleaning process developed in November 1975 for one particular user, and is detailed in Table 3-4, as the alternate procedure. Experimental lot number 9

Table 3-4. Changes in Pre-Epitaxial Cleaning Procedure-November 1975

Standard Procedure Pre-Epitaxy Cleaning	Alternate Procedure Pre-Epitaxy Cleaning
I. Chemical Cleaning	I. Chemical Cleaning
A. Oxidizing acid boil	A. Same
B. D.I. water rinse	B. Same
C. Spin dry in warm dry nitrogen atmosphere.	C. Same
II. Automatic Substrate Scrub	II. Automatic Substrate Scrub
A. Load substrate cartridge into scrubber	A. Same
1. Scrub cycle - brush scrub spinning substrate with detergent-water mixture	1. Same
2. First rinse - dilute NH_4OH rinse	2. Same
3. Second rinse - D.I. water	3. Second rinse - Isopropanol
4. Dry - high-speed spin with blowing dry nitrogen	4. Same
	III. Chemical Cleaning
B. Unload substrate cartridge and store in laminar flow hood.	A. Oxidizing acid boil B. D.I. water rinse
C. Load substrates onto susceptor, using dry, filtered, anti-static nitrogen to blow off surface.	C. Spin dry in warm dry nitrogen atmosphere D. Load substrates onto susceptor, using dry, filtered, anti-static Nitrogen to blow off surface.

generally follows the standard procedure as listed in Table 2-4, except that no detergent or ammonia or alcohol was used in any of the scrubber cycles. Deionized water was the only solvent used in the scrubber. In the following, these variations will be referred to as I, alcohol final rinse, II, alcohol scrub-acid wash, and III, no detergents or organics.

The pre-epitaxial cleaning variations were carried out as shown in Table 3-5, which shows substrate lot selection and experimental conditions for the second experimental set. Epitaxial run identification for the second experimental set is listed in Table 3-6.

Two epi runs were needed to supply five wafers for lot 9. A problem occurred at this time, and deposited films had hazy surfaces. Other substrates from the same lot, KC0084, were selected, cleaned according to instructions, and epi'd. Lot 9 consisted of two wafers from run B12012906 and three wafers from B12013003.

All SOS starting material for Experimental Set II were fabricated in accordance with the standard UCC specifications, with the experimental wafer cleaning variations as the only nonstandard variable (the process variable under study).

Following cleaning, the wafers were spun dry, given the standard hydrogen prefire, and intrinsic (>700 ohm-cm) silicon was grown to a thickness of ~0.75 μm using standard UCC procedures. As with the polishing variations, all films were made in the same reactor (B1200) using the same silane cylinder, by the same operator, during two consecutive days.

3.2 Starting Material Wafer Inspection Results - Lot 618

Pre-processing inspection was conducted using the techniques described in Appendix A. A visual scan of the wafers using the Nomarski filter technique revealed no scratches, pits or bumps in the silicon film. There was no noticeable difference in the general texture of the silicon film from wafer to wafer.

The results of IR spectrophotometer measurements and sodium light topographs, as shown in Table 3-7, showed a typical silicon film thickness variation of 1575 Å--the smallest 1100 Å and the largest 2000 Å. The film was generally found to be thinner at one edge of the wafer and to increase in thickness in a monotonic manner toward the opposite edge. There was no indication of a "ripple effect" of alternately thinner and thicker silicon. The average film thickness on wafers in lot 618 was 0.745 μm.

Table 3-5. Pre-Epitaxial Chemical Cleaning Variations

EXPERIMENTAL SET II

Substrate Lot KC0084

VARIATION I

Select 5 substrates for Exp. Lot No. 7. Do final pre-epitaxial cleaning according to following:
Detergent scrub
NH_4OH rinse
Isopropanol rinse
Spin dry
Load into reactor and deposit films for Lot No. 7

VARIATION II

Select 5 substrates for Exp. Lot No. 8. Do final pre-epitaxial cleaning according to following:
Detergent scrub
NH_4OH rinse
Isopropanol rinse
Spin dry
Oxidizing acid boil
D.I. water rinse
Spin dry
Load into reactor and deposit films for Lot No. 8

VARIATION III

Select 5 substrates for Exp. Lot No. 9. Do final pre-epitaxial cleaning according to following:
No detergent scrub
No NH_4OH rinse
Use H_2O only in scrubber cycles
No Isopropanol rinse
Spin dry
Load into reactor and deposit films for Lot No. 9

Table 3-6. Experimental Set II Identification

Experimental Lot No.	Wafers	Substrate Lot	Experimental Conditions	Epitaxial Run No.
7	5	KC0084	Alcohol Rinse	B12013004
8	5	KC0084	Acid Wash	B12013001
9	5	KC0084	Water Scrub	B12012906 (2) B12013003 (3)

Table 3-7. Wafer Inspection Prior to Device Fabrication

Wafer No.	No. of Fringes	Minimum Thickness, μ	Maximum Thickness, μ
618.1	1.4	0.71	0.82
618.2	2.1	0.67	0.84
618.3	1.8	0.68	0.82
618.4	2.0	0.65	0.81
618.5	2.3	0.64	0.82
618.6	2.1	0.66	0.83
618.7	1.4	0.71	0.82
618.8	1.6	0.68	0.81
618.9	2.2	0.66	0.84
618.10	2.5	0.65	0.85
618.11	1.8	0.68	0.83
618.12	2.4	0.61	0.80

3.3 Device Fabrication - Lot 618

Four wafers from each of the three cleaning variations were processed in one 12-wafer lot, designated lot 618. There were no "standard" wafers in this lot, all having been cleaned using some variation from the standard cleaning procedure. CMOS inverter circuits (4007SR) were fabricated on these wafers as outlined in Appendix B. Processing on this lot was done in the Rockwell Hard MOS Wafer Processing Lab. Due to a malfunction in the ion implanter, the deep boron implant (200 keV) could not be performed in the usual manner. As the implanter would not run at 200 kV, it was set for 100 kV and the ion source set to supply doubly ionized boron instead of the singly ionized boron normally used. Otherwise the process was completely normal. Only one wafer, 618.1, was broken during processing. The wafer numbers corresponding to the different sapphire cleaning variations are tabulated in Table 3-8. The broken wafer is not listed.

Table 3-8. Lot 618 Wafer Identification

Wafer No.	Cleaning Procedure
618.1	I Alcohol final rinse
618.2	"
618.3	"
618.4	"
618.5	II Alcohol scrubber followed by acid wash
618.6	"
618.7	"
618.8	"
618.9	III No detergents or organics
618.10	"
618.11	"

3.4 Wafer Probe Results - Lot 618

The wafers were probed and the resulting data mapped and sorted, and yields were calculated as described in Appendix C. The wafer maps did not show local variations in number or type of failure, except in two cases where a very high leakage current failure rate was noted in one corner of the mapped area of wafer 618.1 and in two corners of wafer 618.11. Because these areas are very near the edges of the wafer, these failures are attributed to handling damage to the wafer.

The yield on the wafers of this lot was much better than the previous lot (610). The yield results are shown in Table 3-9. It is apparent that the alcohol final rinse (cleaning procedure I) is detrimental to the yield of both n- and p-channel transistors, with channel leakage being the major failure mode. Cleaning procedure II (alcohol scrub followed by acid wash) appears to give slightly better yields than III, thus suggesting that the use of detergents and organics is advantageous and that the harmful effects of alcohol are removed by an acid wash. Unfortunately, the limitations of lot size to 12 wafers mitigated against including wafers cleaned with the standard process in this lot, so no yield comparison with the standard clean is made. It was hoped that lot-to-lot processing variations would be sufficiently small to permit some yield comparison with the standard wafers in the other lots, but this was not the case.

The results of sorting the various measurements are shown in the distribution curves of Figures 3-2 to 3-5. As with lot 610, the leakage currents fall either within the rather narrow distributions shown on Figure 3-2 or they are beyond 200 nA. Again the gate leakages were essentially all either less than 200 nA or greater than 2 μA and are not plotted. As only three wafers were tested for cleaning procedure III (no detergents or organics), the distribution curves are lower in height than for procedures I and II where four wafers were tested. The greatest difference between the results of the various cleaning procedures occurs in the voltage drop at 3 mA load where cleaning procedure I (alcohol final rinse) shows a narrower distribution peaked ~50 mV above the other two cases. *In all the above cases, the differences in the measured device parameter values due to the different sapphire cleaning procedures are not great enough to significantly impact device performance.*

Measurements of field-effect mobility were taken at several locations on each wafer using the test devices located between 4007SR dice on alternate rows of the wafer. The results are shown in Table 3-10. Here it appears that cleaning procedure III (no detergents or oganics offers a definite advantage in field-effect mobility in both n- and p-channel transistors.

Table 3-9. Yield Results From Lot 618 - Sapphire Cleaning Variations
Numbers shown are numbers of failures.

SAPPHIRE CLEAN	WAFER NUMBER	FAILED DICE	FAILED INVERTERS	p-CHANNEL	n-CHANNEL	p-CH LEAKAGE	n-CH LEAKAGE	p-CH VOLTAGE	n-CH VOLTAGE	p-CH GATE LEAKAGE	n-CH GATE LEAKAGE
I.	618.1	123	212	185	161	173	134	2	1	12	27
Alcohol	618.2	106	138	106	77	94	58	0	0	11	19
Final	618.3	226	357	308	195	229	82	50	49	28	64
Rinse	618.4	98	116	98	53	93	18	0	2	5	34
	AVERAGE										
	%	46	23	19	13.5	16	8	1.4	1.4	1.6	4
II. Alcohol	618.5	95	114	103	50	95	20	2	3	8	30
Scrub-	618.6	153	204	194	75	180	22	3	2	14	53
Acid	618.7	80	90	82	26	78	7	1	2	4	18
Wash	618.8	63	76	45	48	42	36	2	2	3	12
	AVERAGE										
	%	32.5	13.4	11.7	5.5	10.9	2.4	0.2	0.25	0.8	3.1
III. No	618.9	66	87	61	54	57	41	0	3	4	13
Detergents	618.10	107	139	120	67	114	36	2	2	5	31
or	618.11	133	194	170	126	156	96	1	1	14	30
Organics											
	Average										
	%	34	15.5	13	8.5	12.1	6.4	0.11	0.22	0.85	2.7

Failure criteria: channel leakage $>10^{-7}$ amps at V_{DS} = 10V, voltage drop >0.5V at 3 ma load, and gate leakage $>10^{-6}$ amps at V_{GS} = 10V.

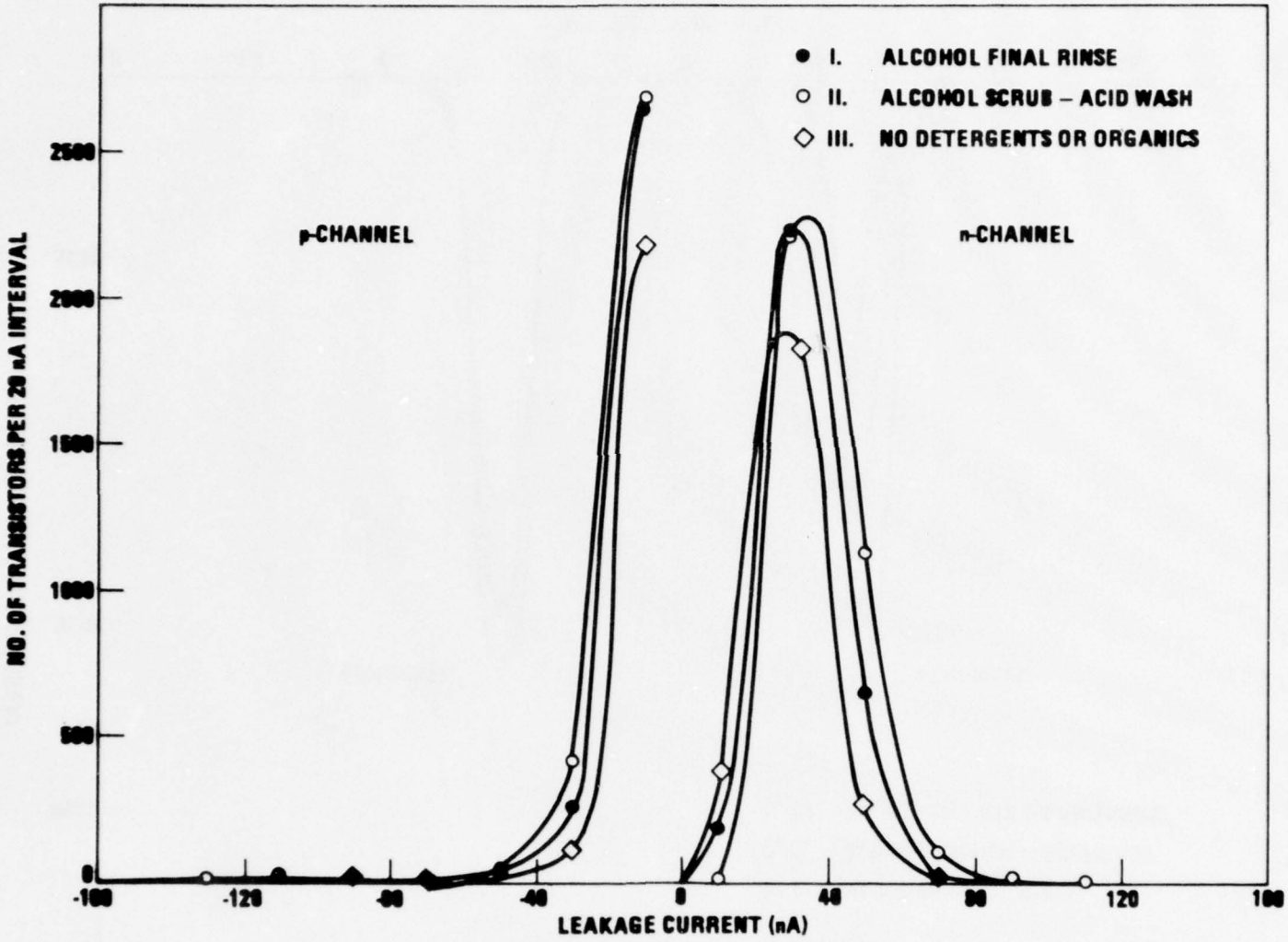

Figure 3-2. Effect of Sapphire Cleaning on Drain Leakage

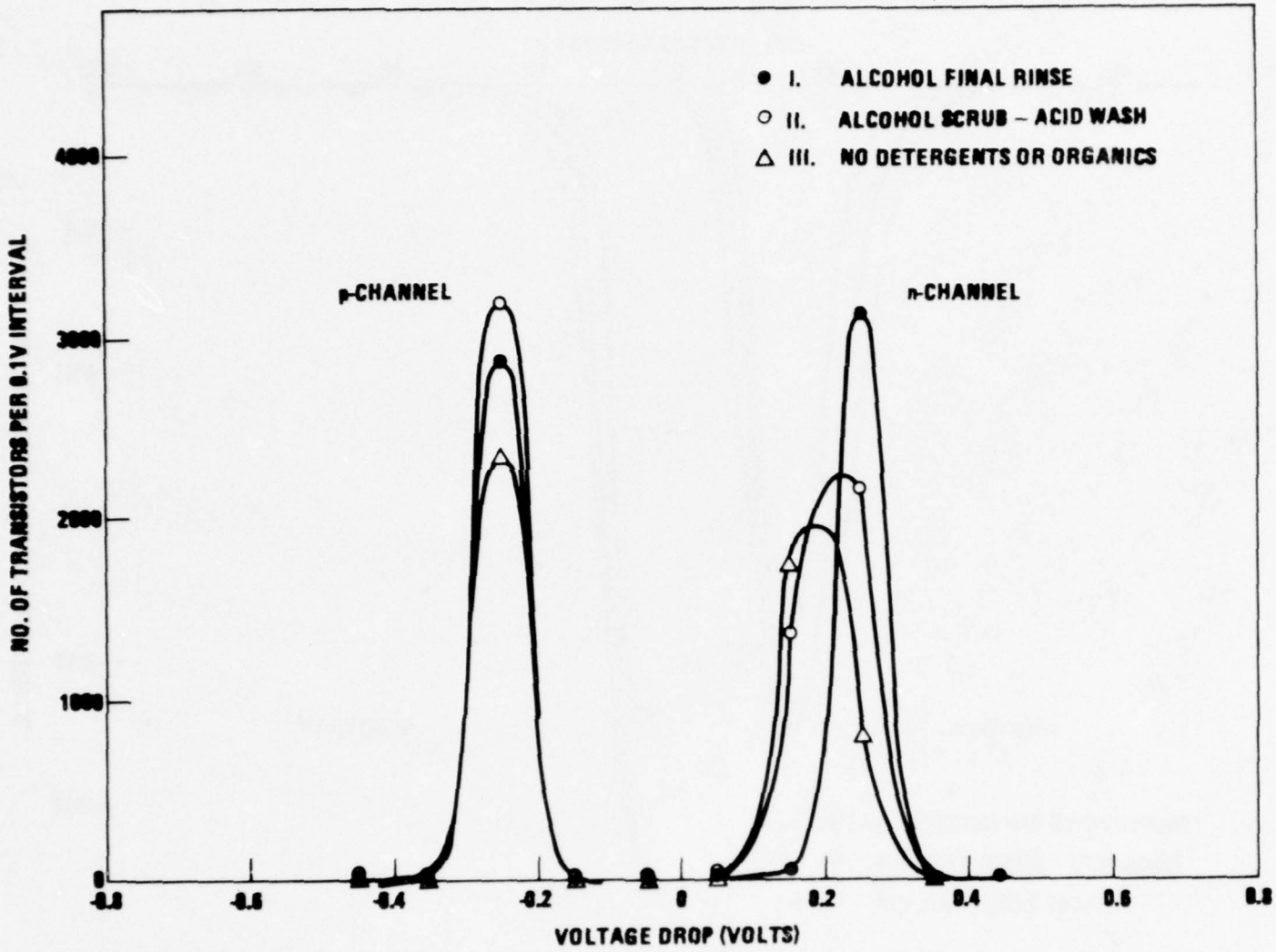

Figure 3-3. Effect of Sapphire Clean on Voltage Drop

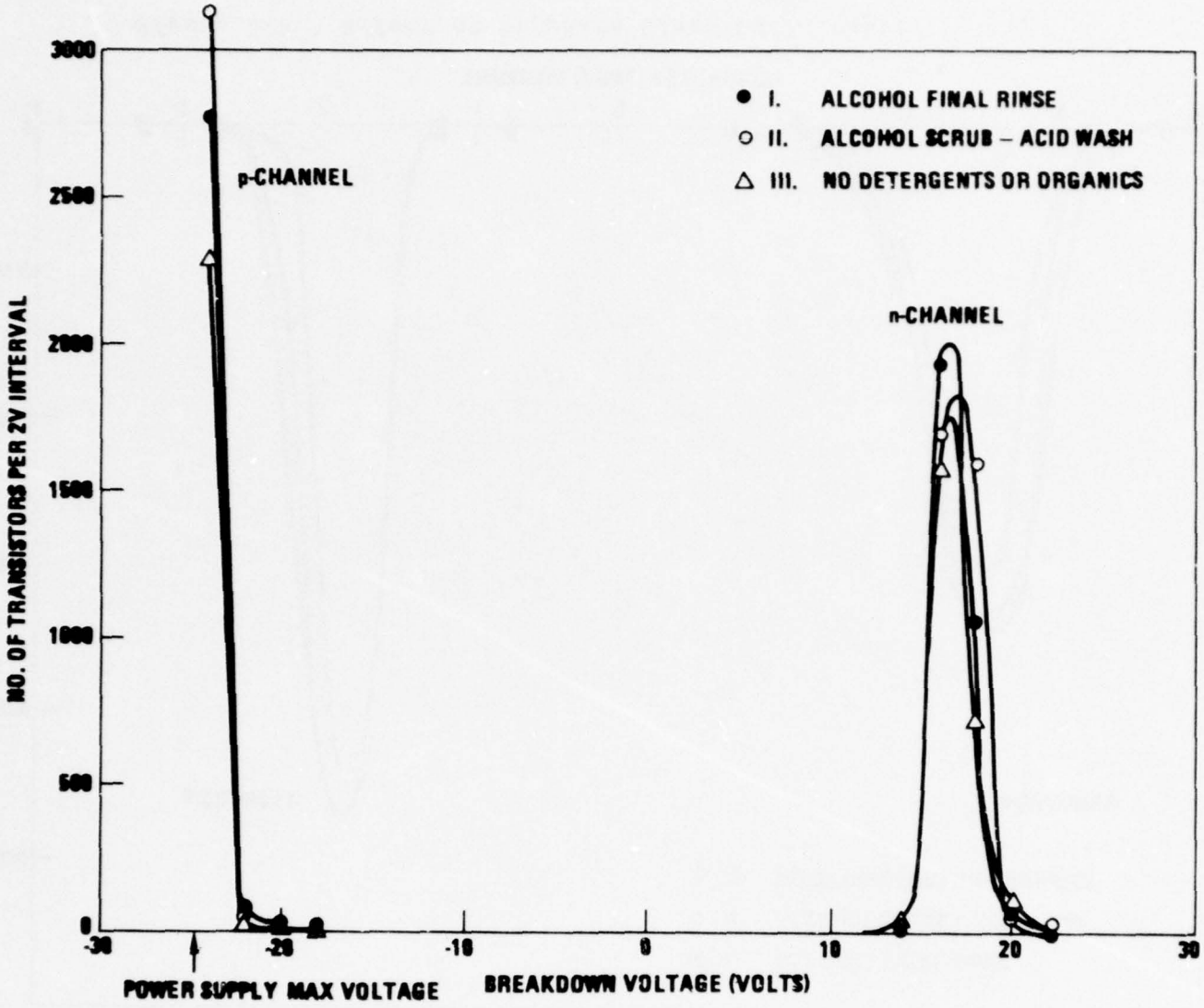

Figure 3-4. Effect of Sapphire Clean on Breakdown Voltage

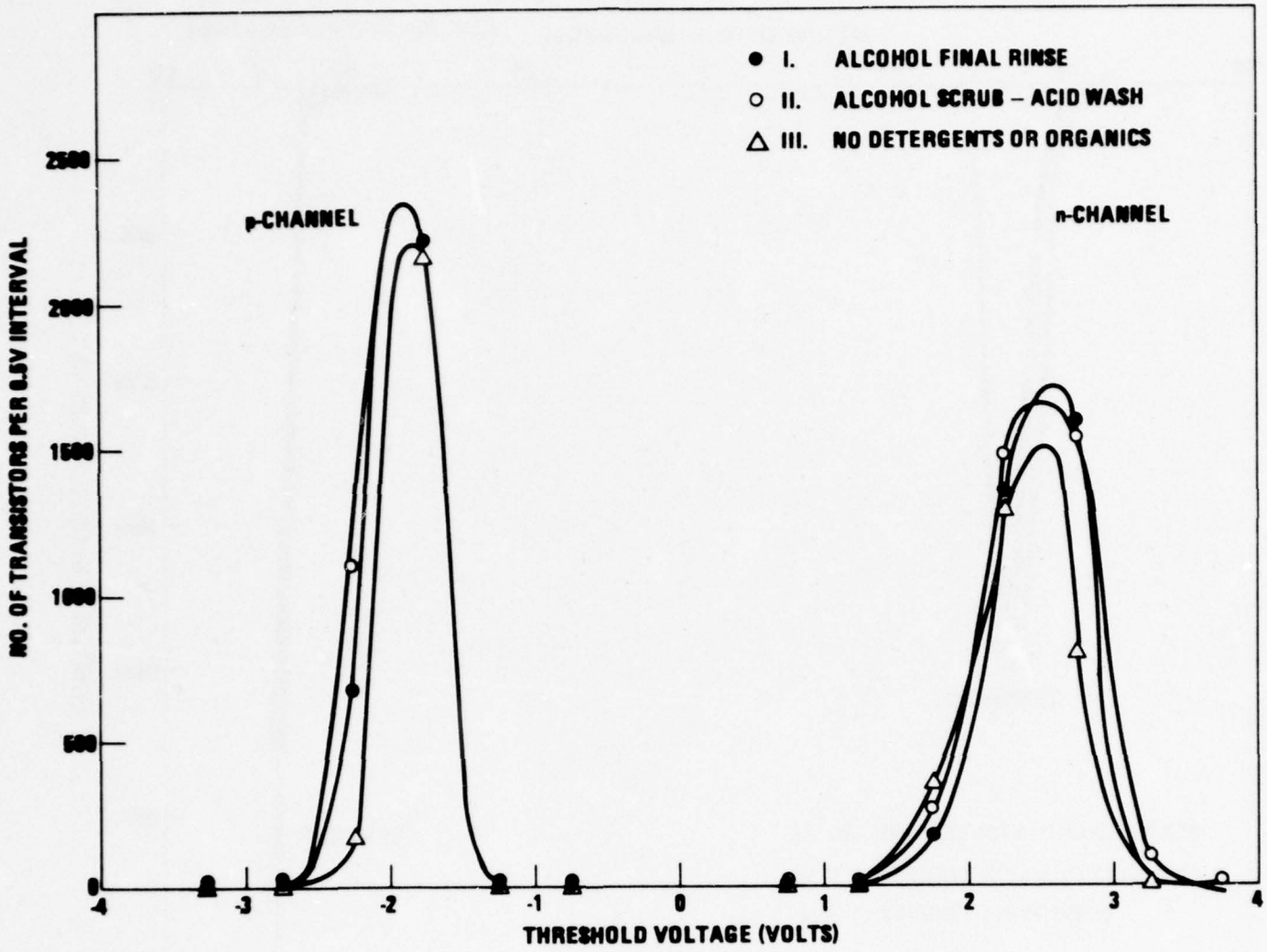

Figure 3-5. Effect of Sapphire Clean On Threshold Voltage

Table 3-10. Effect of Sapphire Cleaning on Field-Effect Mobility

Sapphire Clean	Wafer Number	Average Field-Effect Mobility ($cm^2V^{-1}sec^{-1}$) p-channel	n-channel
I	618.1	225.0	405.5
Alcohol	618.2	244.2	353.6
Final	618.3	232.5	340.5
Rinse	Average	233.9	366.5
II	618.5	196.7	408.8
Alcohol	618.6	192.8	387.1
Scrub-	618.7	197.1	410.5
Acid	618.8	193.7	388.6
Wash	Average	195.1	398.8
III	618.9	301.1	485.4
No	618.10	232.3	361.8
Detergents	618.11	257.5	416.1
or Organics	Average	263.6	421.1

3.5 Stability in Co^{60} Environment - Lot 618

The Co^{60} testing was done as described in Appendix D. Dice to be tested were selected on the basis of the failure maps generated from the wafer probe data and were taken from three locations on each wafer to examine the effects of Si film thickness. Radiation-induced threshold shifts are shown in Table 3-11 for the different sapphire cleaning variations. The numbers shown are the average of three devices for each wafer and are the maximum shift observed, which usually, but not always for n-channel transistors, occurred at the maximum dose used (10^6 rads). The threshold shifts for lot 618 are all somewhat less than for lot 610, indicating better processing on lot 618. The results of Table 3-11 indicate that cleaning procedure III (no detergents or organics) leads to a slight improvement in radiation-induced threshold shift on p-channel transistors over the other two cleaning procedures. This advantage is only on the order of 10% and is somewhat questionable, in view of the poor statistics in the case of positive bias where there are results from only two wafers using cleaning procedure III.

Radiation-induced n-channel leakage currents are shown in Table 3-12. The maximum leakage current (measured at V_{GS} = -10 V, V_D = +10 V) often occurred at doses below 1 megarad, in which cases the maximum value is tabulated instead of the 1 megarad value. The maximum leakage current always occurred at a radiation bias of V_D = +10 V, V_{GS} = 0. Also shown is the initial thickness of the silicon film at the location on the wafer from which the device was taken. In terms of radiation-induced leakage, the cleaning procedures are clearly ranked II, III, I,

Table 3-11. Effect of Sapphire Clean on Radiation-Induced Threshold Shift

Sapphire Clean	Wafer Number	N-Channel ΔV_T V_G = -10 V	N-Channel ΔV_T V_G = +10 V	P-Channel ΔV_T V_G = -10 V	P-Channel ΔV_T V_G = +10 V
I	618.1	-0.08	-0.58	-0.57	-2.42
Alcohol	618.2	-0.06	-0.21	-0.39	-1.60
Final	618.3	-0.08	-0.58	-0.58	-2.12
Rinse	618.4	-0.05	-0.27	-0.47	-2.19
	Average	-0.07	-0.55	-0.50	-2.08
II	618.5	-0.05	-0.26	-0.49	-2.31
Alcohol	618.6	-0.11	-0.52	-0.72	-2.49
Scrub-	618.7	-0.10	-0.49	-0.60	-2.12
Acid	618.8	-0.09	-0.18	-0.40	-1.55
Wash	Average	-0.09	-0.36	-0.55	-2.12
III	618.9	-0.07	-0.23	-0.37	-1.55
No	618.10	-0.07	-0.42	-0.53	-2.13
Detergents	618.11	-0.08	-0.37	-0.46	-
or Organics	Average	-0.07	-0.34	-0.45	-1.84

with II (alcohol scrub followed by acid wash) giving a factor of four less leakage than I (alcohol final rinse). It is interesting to note that while the maximum radiation-induced leakage is usually a decreasing function of silicon film thickness (as in lot 610), this was not the case for wafers 618.1, 618.3, and 618.6. In the first two cases, inspection of the drain current versus gate voltage curies showed that while the leakage at 0.1 V on the drain did show the normal leakage versus silicon thickness behavior, the measurements at a drain voltage of 10 V showed the reverse behavior.

To further understand the anomalous leakage current behavior, on all the subsequent measurements (following 618.3), the n-channel leakage current was measured as a function of drain voltage with V_{GS} = -10 V following each radiation exposure. A result typical of wafer 618.4 is shown in Figure 3-6. The striking feature of these curves is that the 3×10^5 rads curve completely lost the shape characteristic of a normal channel, but that the normal shape returned to the curve after 10^6 rads. This behavior was not seen on wafers from the other two cleaning procedures, and is believed to be due to impurities left at the silicon-sapphire interface by the alcohol final rinse.

Table 3-12. Effect of Sapphire Clean on Radiation-Induced Leakage

Sapphire Clean	Wafer	Device	Leakage(μA)	Dose(rads)	Si Thickness (μm)
I	618.1	2008	259	3×10^5	.73
Alcohol		2020	183	1×10^6	.78
Final		2130	308	1×10^6	.80
Rinse	618.2	0720	15.9	3×10^5	.83
		2018	75	1×10^6	.78
		3118	181	1×10^6	.71
	618.3	2008	261	1×10^6	.80
		2120	152	1×10^6	.78
		2130	235	1×10^5	.74
	618.4	0708	685	1×10^5	.65
		1720	220	1×10^5	.72
		3130	118	1×10^5	.78
	Average		224		
II	618.5	0708	74.4	1×10^5	.64
Alcohol		2020	46.6	1×10^5	.75
Scrub-		3130	47.4	1×10^5	.78
Acid	618.6	0730	52.1	3×10^5	.81
Wash		2030	37.0	1×10^6	.72
		3030	10.4	1×10^6	.67
	618.7	2008	123.6	1×10^6	.72
		2020	93.6	1×10^6	.77
		2030	113.9	1×10^6	.79
	618.8	0720	8.6	1×10^6	.80
		2020	17.7	1×10^6	.75
		3020	34.6	1×10^5	.70
	Average		55		
III	618.9	0720	252	1×10^5	.67
No		2020	103	1×10^6	.80
Detergents		3120	36.2	1×10^6	.83
or	618.10	0710	177	1×10^6	.65
Organics		1414	107.5	3×10^5	.73
		1818	77.4	3×10^5	.78
		2424	48.0	1×10^6	.82
		3026	12.1	1×10^6	.85
	618.11	2008	78.2	3×10^5	.79
		2118	134	1×10^6	.76
		2030	237	1×10^5	.71
	Average		140		

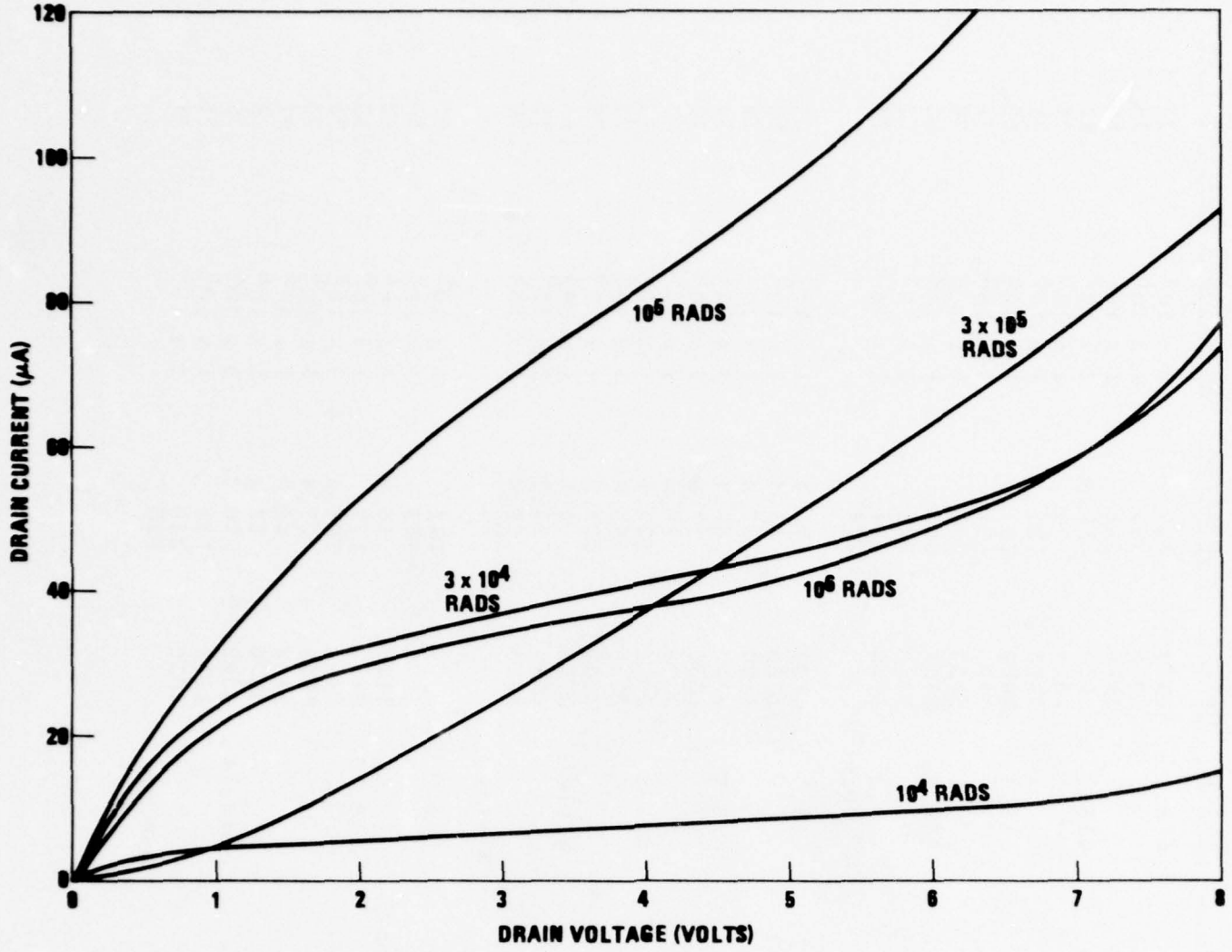

Figure 3-6. Radiation Induced N-Channel Leakage Characteristics for Device 1720 on Wafer 618.4 (I. Alcohol Final Rinse)

3.6 Stability Under Bias-Temperature Stress - Lot 618

These measurements were done on two dice from each wafer as described in Appendix E. The results are summarized in Table 3-13. Although changes induced by the bias temperature stress were small, they were larger for both cleaning procedures I and II and smaller for cleaning procedure III than had been observed for the wafers using the standard cleaning procedure in the polishing variation experiments. Also for cleaning procedure II (alcohol scrub - acid wash), a considerable number of transistors were destroyed (loss of transistor action) by the bias temperature stress. Thus, it is apparent that cleaning procedure III is distinctly superior to either I or II under B-T stress. While it is clear that the alcohol final rinse is detrimental to the bias temperature stability in regard to threshold voltage shift, transconductance, and drain leakage, it is not clear whether it is the use of alcohol or the use of the acid as a final wash which has led to the poor results of cleaning procedure II. It is felt that the single device from wafer 618.11 exhibiting a very high drain leakage following B-T stress should be regarded as an anomally and that cleaning procedure III is the preferred one from the bias-temperature standpoint.

3.7 Sapphire Clean Results

The most definite feature of the sapphire clean data is that cleaning procedure I (alcohol final rinse) yields the least desirable results on most parameters measured--namely, yield, voltage drop, n-channel field-effect mobility, radiation-induced threshold voltage shift, on n-channel transistors, and radiation induced n-channel leakage. The choice between cleaning procedures II and III then rests with which parameters are considered most important. Thus, cleaning procedure II (alcohol scrub followed by an acid wash) provided slightly better yield and significantly lower radiation-induced n-channel leakage than III, while giving the lowest p-channel field-effect mobility and highest p-channel threshold shift of the three cleaning procedures, and exhibiting inferior stability plus some complete failures under bias-temperature stress. Cleaning procedure III (no detergents or organics), on the other hand, provided the best field-effect mobility for both n- and p-channel transistors and also showed the lowest radiation-induced threshold voltage shifts and best bias-temperature stability. From the standpoint of radiation hardening, however, the radiation-induced n-channel leakage advantage of cleaning procedure II would outweigh the small threshold shift advantage of cleaning procedure III. No comparison with the standard cleaning procedure could be made due to processing variations in other lots where standard wafers were included.

In general, it appears that cleaning procdure I is detrimental to n-channel transistors, while cleaning procedure II is somewhat detrimental to p-channel transistors and generally beneficial to

Table 3-13. Effect of Sapphire Clean on Bias-Temperature Stability

SAPPHIRE CLEAN	WAFER NUMBER	DEVICE NUMBER	MAXIMUM THRESHOLD SHIFT			MAXIMUM TRANSCONDUCTANCE LOSS			MAXIMUM DRAIN LEAKAGE		
			ΔV_T(VOLTS)	TYPE	BIAS	ΔG_M %	TYPE	BIAS	I_{DL}(μA)	TYPE	BIAS
I.	618.3	2126	-0.25	N	1	25	P	1	0.47	N	2
Alcohol		2124	-0.7	N	1	46	P	1	3.82	N	2
Final	618.4	2020	-0.7	N	1	48	P	1	3.98	N	2
Rinse		1920	-0.4	N	1	26	P	1	3.43	N	2
		1820	-0.8	N	1	41	P	1	8.27	N	2
II.	618.5	1818	-0.15	N	2	–	–	–	0.78	N	2
Alcohol		1618	-0.25	N	1	25	P	1	4.71	N	1
Scrub	618.6	2330	-0.6	N	2	20	P	1	1.93	N	2
Acid		2130	-0.25	N	1	25	P	1	3.03	N	2
Wash	618.7	2122	-0.25	N	2	20	P	2	2.17	N	2
		2022	-0.67	N	2	35	P	2	17.37	P	1
	618.8	2220	-0.5	N	1	45	P	2	5.85	N	2
		2120	-0.15	N	2	10	N	2	1.75	N	1
III.	618.9	2220	-0.3	N	1	37	P	1	1.15	N	2
No		2120	-0.3	N	1	21	P	1	2.68	N	2
Detergents	618.10	2018	-0.12	P	2	0	–	–	0	–	–
or		2020	-0.12	P	2	0	–	–	0	–	–
Organics	618.11	2020	-0.12	P	2	0	–	–	0	–	–
		2120	-0.12	P	2	0	–	–	239	N	1

n-channels. In any case, it is apparent that the detrimental effects of alcohol in the cleaning procedure are largely removed by the use of an acid final wash. The acid final wash may offer its own advantages in terms of the silicon-sapphire interface, possibly etching the sapphire somewhat or removing polishing debris to produce a roughened surface. This would be in agreement with the sapphire polish findings where the inferior polish produced the best n-channel transistors. Unfortunately, the scope of this program is not sufficient to include combinations of polish and cleaning to see if, for example, the apparent advantages of a slightly rough sapphire surface in terms of back-channel effects on n-channel transistors could be combined with the advantages of removing detergents and organics in terms of field-effect mobility and radiation-induced threshold shifts.

4. HYDROGEN PREFIRE AND ANNEALING EXPERIMENTS

In the standard UCC SOS fabrication procedure, the last treatment of the sapphire before silicon growth is an annealing step in the presence of hydrogen gas. This step is usually known as hydrogen prefire. The purpose of the prefire step is to etch off a small amount of the sapphire wafers, removing material damaged during polishing, and providing a fresh surface upon which to grow the epitaxial silicon. In order to establish the optimum degree of prefire, it was decided to examine the effect of different hydrogen prefire times on SOS material quality. Also, it was decided to investigate the effect of a second annealing step, in the presence of a different gas, in addition to the normal hydrogen prefire. The additional annealing step was viewed as a supplementary cleaning process, and so occurred after the regular cleaning procedure and immediately before the hydrogen prefire. The annealing ambients chosen were HCl gas and oxygen gas, each of which is expected to react with different types of impurities.

The SOS wafers used in these experiments were from the second group of wafers described in Table 1-2. This group incorporated four variations in the pre-epitaxial annealing procedure including two variations in the duration of the hydrogen anneal or prefire and two variations in the gas ambient in an additional annealing step. The standard hydrogen prefire cycle is carried out in the same reactor as the silicon growth for a period of five minutes at a temperature of 1150°C. This first variation on this procedure was to extend the duration to 30 minutes, and the second variation was to reduce the time to zero minutes. The third variation was to anneal the sapphire substrates in an atmosphere of oxygen (O_2) for 16 hours at 1100°C immediately before placing them in the reactor for a normal (5-minute) hydrogen prefire and silicon epitaxy. The fourth variation was to place the sapphire substrates in the reactor and treat them in HCl gas at 800°C and two litres per minute for a period of two minutes prior to a normal hydrogen prefire and silicon epitaxy.

All the films in the second group were made by the same operator in the same reactor (A1200), using the same silane cylinder and on consecutive days. The reactor and silane cylinder were both different than used for the first group of wafers. Two different sapphire boules were used in the second group of wafers. For each of the four pre-epitaxial anneal variations, five wafers were taken from boule KC0084 and seven were from boule KC00133. Since all the wafers from the first group were from boule KC0084, the experiments described in this section were also done on wafers from this boule. As before, the silicon films were intrinsic and ~0.75 μm thick.

4.1 Hydrogen Prefire Experiments

4.1.1 Technical Approach and Rationale

Several years ago, long high-temperature prefires were necessary to remove polishing damage in the substrate, in order to deposit single-crystal films. As polishing techniques developed, polishing damage was minimized, allowing shorter, lower temperature prefiring cycles. With the development of the chemical-mechanical polish, it was found that hydrogen prefires were not necessary to obtain high-quality, single-crystal silicon films.

At Union Carbide, the hydrogen prefire has always been a part of the standard epitaxial procedure. The time and temperature have been reduced as the polishing quality has improved. The prefire has been retained as it is felt that it performs a beneficial light etch and cleaning step. Various experiments have been made in cooperation with several SOS users, attempting to determine the effect of eliminating the prefire cycle on device parameters. These experiments were not conclusive, and it is felt that other parameters, probably surface cleanliness, interfered with these tests. One user has requested that Union Carbide continue to supply wafers using a hydrogen prefire of at least five minutes at 1150°C. This user insists on a hydrogen prefire, as he has identified this as critical to device performance. He states that several lots of wafers received from another vendor gave devices with unacceptable electrical properties. Investigation revealed that this vendor had not used a hydrogen prefire cycle when making these wafers. Correspondingly, wafers from Union Carbide gave devices with acceptable electrical properties, having been prepared with the standard prefire cycle. At that time, the hydrogen prefire cycle used at Union Carbide was 5 minutes at 1150°C. This cycle was established as standard and has been continued through the present time.

It was felt that the prefire cycle should be examined in this program and wafers were fabricated with variations of time and temperature. It has been postulated that the hydrogen prefire contributes to autodoping of Al into the silicon film, especially during the first stages of nucleation and growth. The effect of the prefire cycle on device parameters has not been reported, and it was hoped that this program might indicate the relative importance of the prefire.

The substrate lot selection and variations in hydrogen prefire conditions are given in Table 4-1. Epitaxial run identification for this third experimental set is listed in Table 4-2.

The hydrogen prefire cycle is done in the same reactor used for film deposition. Deposition immediately follows the prefire cycle, so that substrates are not exposed to any atmosphere other than hydrogen from the start of the prefire cycle to post-deposition cooling. In practice, substrates are loaded onto the susceptor in

Table 4-1. Hydrogen Prefire Variations

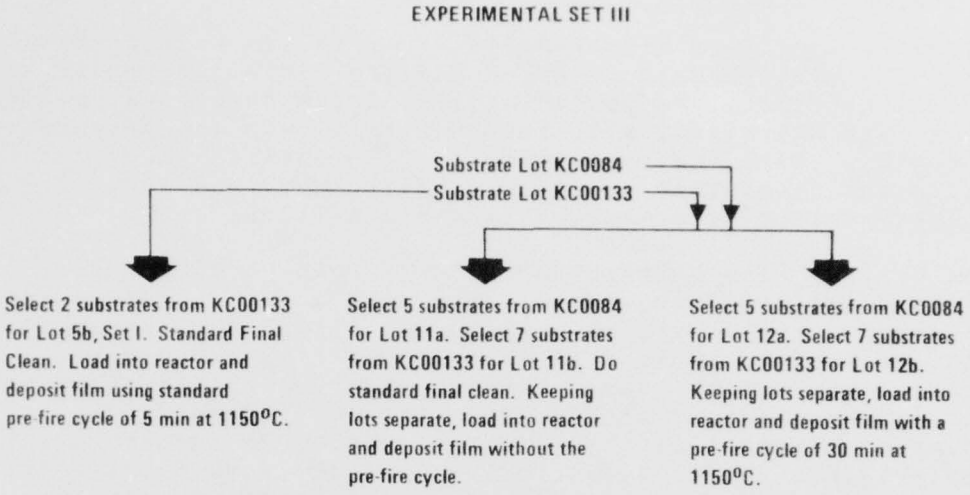

Table 4-2. Experimental Set III Identification

Exp. Lot No.	Wafers	Substrate Lot	Exp. Conditions	Epitaxial Run No.
5b	2	KC00133	Standard	A12050605
11a	5	KC0084	No pre-fire	A12050508
11b	7	KC00133	No pre-fire	A12050603
12a	5	KC0084	30 min. at 1150°C	A12050506
12b	7	KC00133	30 min. at 1150°C	A12050611

the reactor. A bell jar covers the susceptor and nitrogen is used to purge all entrapped air from the system. After the purge, hydrogen is introduced, at flow rates approaching 80 liters per minute. The substrates are heated to 1150°C, held at temperature for the specified time, then cooled in the hydrogen atmosphere to the deposition temperature, and the silicon film is deposited. After deposition, films are partially cooled in the hydrogen atmosphere, then the atmosphere is changed to nitrogen, until all hydrogen is purged out and the bell jar can be opened to air.

Except for the prefire step, all wafers delivered for experimental Set III were fabricated in accordance with the standard UCC specifications.

4.2 Annealing Experiments

4.2.1 Technical Approach and Rationale

The silicon-sapphire interface has been identified as extremely important to device performance. Previous experiments were designed to study surface finish quality, cleanliness, and pre-fire effects on the substrate surface and subsequent interface quality. Those experiments used variations of standard quality or procedures currently in use. For this set of experiments, termed annealing experiments, new areas were investigated that are not currently a part of the standard wafer fabrication process.

Two approaches were attempted to change the surface conditions at the interface. One approach was to expose the substrate to an oxidizing atmosphere, just prior to film deposition. It was thought that this atmosphere may affect the chemistry of the surface, providing an oxygen-rich composition that would favorably affect film nucleation. In addition, it was thought that any organic residues on the surface would be oxidized by this atmosphere, providing very clean surfaces prior to epitaxy. Oxygen was chosen, since it should be most efficient.

The other approach was to expose the substrate to reducing atmosphere prior to film deposition. This atmosphere should also affect the chemistry of the surface, providing an oxygen-deficient surface and affecting film nucleation. Additionally, this reducing atmosphere would provide cleaning action just prior to epitaxy that would be quite different from the oxidizing atmosphere. Gaseous hydrogen chloride was chosen as the reducing atmosphere, since it effectively etches sapphire above 900°C. HCl is also used in the semiconductor industry as a getter for sodium contaminants on surfaces, so that an HCl pre-epi anneal should provide a sodium-free sapphire surface and film interface.

Four lots were fabricated with oxygen and HCl annealing cycles. Oxygen annealing was done in a diffusion furnace at 1100°C for 16 hours. The substrates were then transferred to the reactor for deposition. HCl annealing was done in the epitaxial reactor just prior to film deposition, so that the substrates were not exposed

to oxygen prior to film deposition. A temperature of 800°C was chosen as tests showed that this would avoid the heavy etching action and deteriorations of surface finish quality, while providing cleaning action.

The substrate lot selection and annealing conditions are given in the flow chart of Table 4-3. Epitaxial run identification for this fourth experimental set is listed in Table 4-4.

Table 4-3. Annealing Experiments

EXPERIMENTAL SET IV

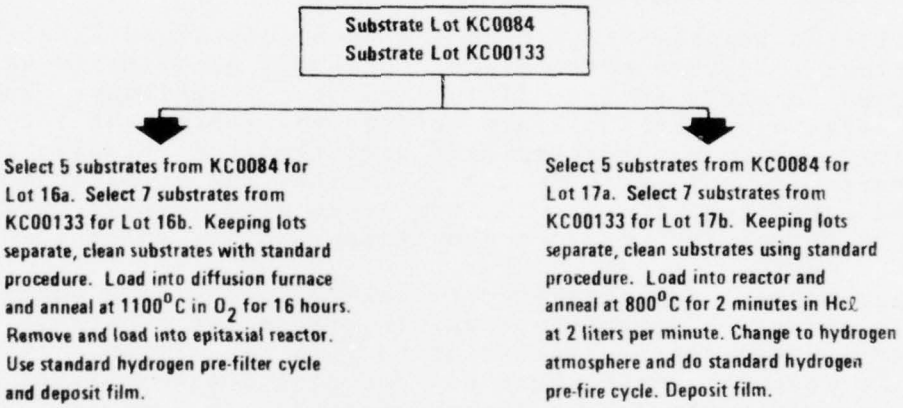

Table 4-4. Experimental Set IV Identification

Exp. Lot No.	Wafers	Substrate Lot	Exp. Conditions	Epitaxial Run No.
16a	5	KC0084	16 hr. in O_2 at 1100°C	A12050608
16b	7	KC00133	16 hr. in O_2 at 1100°C	A12050607
17a	5	KC0084	2 min. in HCl at 800°C	A12050609(2) A12050612(3)
17b	7	KC00133	2 min. in HCl at 800°C	A12050606

Two epitaxial runs were necessary to complete lot 17a. Some substrates selected for this run were later found to have been contaminated during cleaning, leaving smears and boat marks. Other substrates were selected and used to complete the lot. Two (2) wafers from A12050609 were used; the remainder (3 wafers) were from A12050612.

The oxygen annealing was done in a quartz tube diffusion furnace. Dry, pure oxygen was used at a flow rate of 15 cubic feet/hour. Substrates were heated at 1100°C and held at temperature for 16 hours. After cooling, the substrates were loaded into the epitaxial reactor and taken through the standard hydrogen prefire cycle prior to film deposition.

The hydrogen chloride annealing was done in the epitaxial reactor. Substrates were loaded into the reactor, heated to 800°C while in a hydrogen atmosphere, then gaseous HCl was introduced at a flow rate of 2 liters per minute. After 2 minutes, the flow of HCl was extinguished, and the heating continued in hydrogen through the prefire cycle and film deposition.

Except for the anneal step, all wafers delivered for Experimental Set IV were fabricated in accordance with the standard UCC specifications.

4.3 Starting Material Wafer Inspection Results - Lot 627

Pre-processing inspection was conducted using the techniques described in Appendix A. A visual scan of the wafers using the Nomarski filter technique revealed no scratches, pits or bumps in the silicon film. There was no noticeable difference in the general texture of the silicon film from wafer to wafer.

The results of the IR spectrophotometer measurements and sodium light topographs, as shown in Table 4-5, showed a typical silicon film thickness variation of 700 Å, the smallest 200 Å, and the largest 1800 Å. The film was generally found to be thinner at one edge of the wafer and to increase in thickness in a monotonic manner toward the opposite edge. There was no indication of a "ripple effect" of alternately thinner and thicker silicon. The average film thickness on wafers in lot 627 was 0.798 μm.

Table 4-5. Wafer Inspection Prior to Device Fabrication

Wafer No.	No. of Fringes	Minimum Thickness (μm)	Maximum Thickness (μm)
627.1	0.4	0.85	0.88
.2	0.4	0.83	0.85
.11	0.6	0.79	0.84
.12	0.5	0.81	0.85
627.3	0.9	0.75	0.82
.4	0.8	0.78	0.84
.13	0.4	0.83	0.86
.14	1.0	0.72	0.90
627.5	0.4	0.86	0.89
.6	1.1	0.77	0.86
.15	0.4	0.84	0.87
.16	0.5	0.83	0.87
627.7	1.2	0.73	0.83
.8	1.1	0.75	0.84
.17	0.4	0.73	0.76
.18	1.7	0.73	0.87
627.9	0.9	0.65	0.72
.10	2.0	0.64	0.80
.19	1.1	0.65	0.74
.20	1.0	6.70	0.78

4.4 Device Fabrication - Lot 627

Four wafers of each of the four pre-epitaxial annealing variations plus four standard wafers (from the first group of wafers received from UCC) were processed in a 20-wafer lot designated lot 627. Only wafers from substrate lot KC0084 were used. CMOS inverter circuits were fabricated on these wafers as outlined in Appendix B. Since some processing steps were limited to a maximum of 12 wafers, the 20 wafers were split into two groups of ten with two wafers from each of the five variations in each group, as shown in Table 4-6. Processing steps which could accommodate all 20 wafers were done with all the wafers at once, while steps which were limited to less than 20 wafers were done in the two separate groups of ten. Because of repairs being done on the n^+ diffusion furnace, the n^+ diffusions were done in the Rockwell Advanced Device Research Lab, while the other processing steps were done in the Rockwell Hard MOS Processing Lab. Only one wafer, 627.12, was broken during processing, and it was not used in the characterization experiments. The use of a faulty metal mask led to an open circuit between the source pad and source contact metal on the middle n-channel transistor on each die on every wafer of this lot.

Table 4-6. Lot 627 Wafer Identification

Wafer No.	Pre-Epitaxial Anneal	Processing Subgroup
627.1	No Prefire	A
627.2	" "	A
627.11	" "	B
627.12	" "	Broken
627.3	30-Minute H_2 Prefire	A
627.4		A
627.13		B
627.14		B
627.5	16-Hour O_2 Anneal	A
627.6	followed by	A
627.15	Standard H_2 Prefire	B
627.16		B
627.7	2-Minute HCl Anneal	A
627.8	followed by	A
627.17	Standard H_2 Prefire	B
627.18		B
627.9	Standard H_2 Prefire	A
627.10	(5 minute)	A
627.19		B
627.20		B

4.5 Wafer Probe Results - Lot 627

The wafers were probed and the resulting data mapped and sorted as described in Appendix C. Because of some pecularities, the parameter distributions will be discussed first. The results of sorting the measurements are shown in the distribution curves of Figures 4-1 to 4-4. The leakage current distributions indicate some lowering of n-channel leakage by all three annealing procedures which involved additional annealing beyond the normal five-minute hydrogen prefire. The least lowering was obtained with the 30-minute hydrogen prefire, while the most lowering (~15 nA) was obtained with the 16-hour oxygen anneal. In the leakage current distribution curves as in all the other lot 627 parameter distribution curves, the lower height of the n-channel curves, compared with the p-channel curves, reflects the fact that one-third of the n-channels were not operational due to use of a faulty metal mask, leading to no connection between the source contact and the source pad. Likewise, the lower height of the curves for devices having no prefire compared to the other curves reflects a lower yield of both n- and p-channels for the no prefire case.

The voltage drop distributions are shown in Figure 4-2 and indicate significantly higher voltage drops than encountered in the other two device fabrication lots (610 and 618). Thus, for all pre-epitaxial anneal cases, a significant fraction of the n-channels exceeded 0.5 V voltage drop, which was the failure level assumed in previous yield analyses. This is particularly striking in the case of the HCl anneal where there are two distinct peaks in the distribution curve. The lower peak is associated with wafers 627.8 and 627.17, while the upper peak is associated with wafers 627.7 and 627.18. Examination of the conductance vs. gate voltage curves for devices from these wafers indicates a rapid decrease in transconductance as the gate voltage increases above 3 volts. Transconductance below V_{GS} = 3 V was normal. This phenomenon was not observed on any of the other wafers.

Distributions of the other parameters were not very different for the five pre-epitaxial annealing procedures. On breakdown voltage, the median of the distribution for the standard prefire case was a little higher (~2 V) than for the other wafers, however, which might reflect the fact that the standard wafers were from the first group of wafers received from Union Carbide, while the wafers for the other four pre-epitaxial anneal conditions were from the second group. On threshold voltage, the HCl anneal gave a somewhat narrower distribution for the n-channel transistors. These differences are probably not important as far as device performance is concerned.

Due to the abnormally high values of voltage drop, which occurred for the standard wafers as well as the wafers having variations in the pre-epitaxial annealing procedure, it was decided to increase the failure threshold for voltage drop to 0.8 V for the

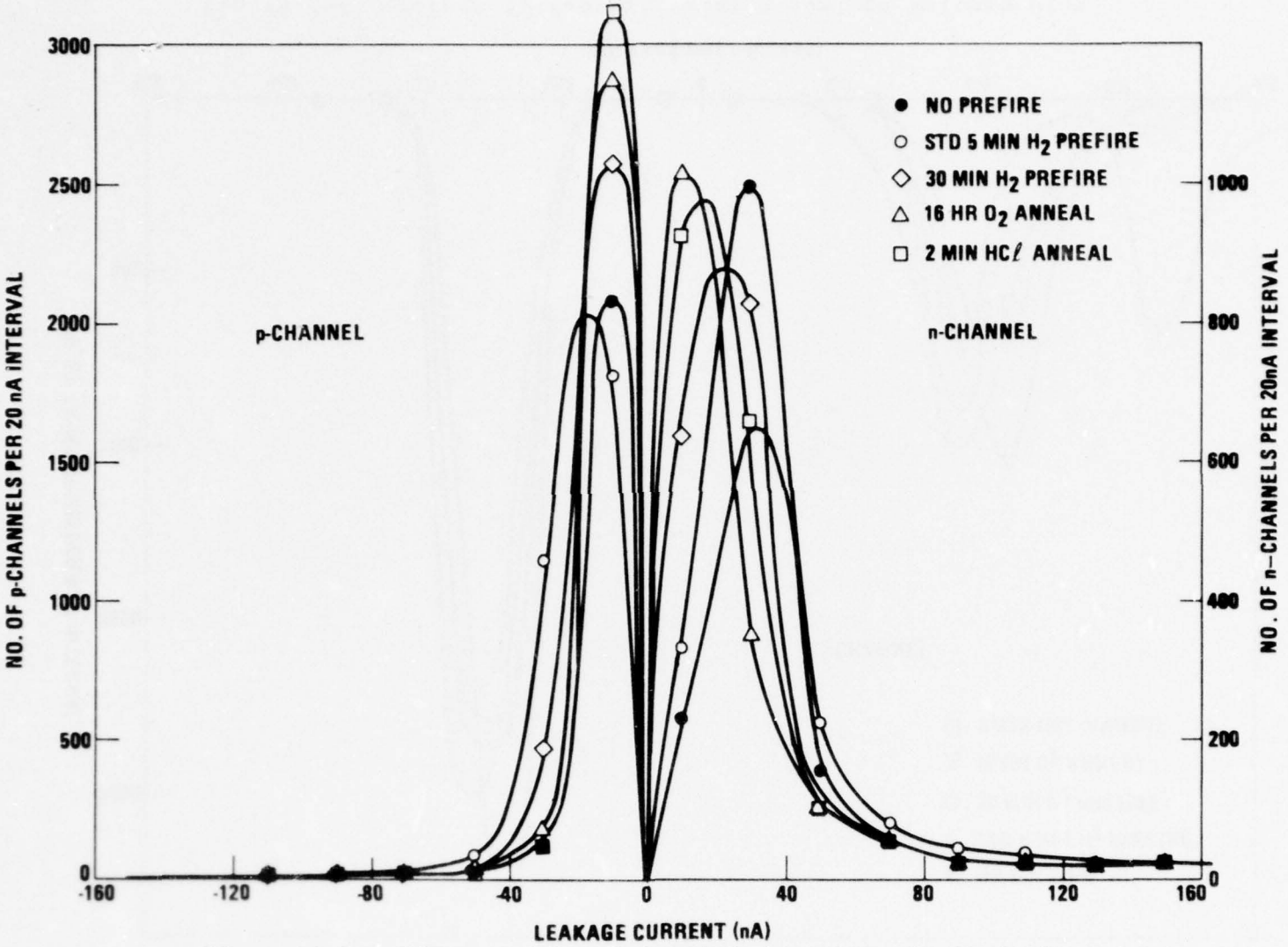

Figure 4-1. Effect of Pre-Epitaxial Anneal on Drain Leakage

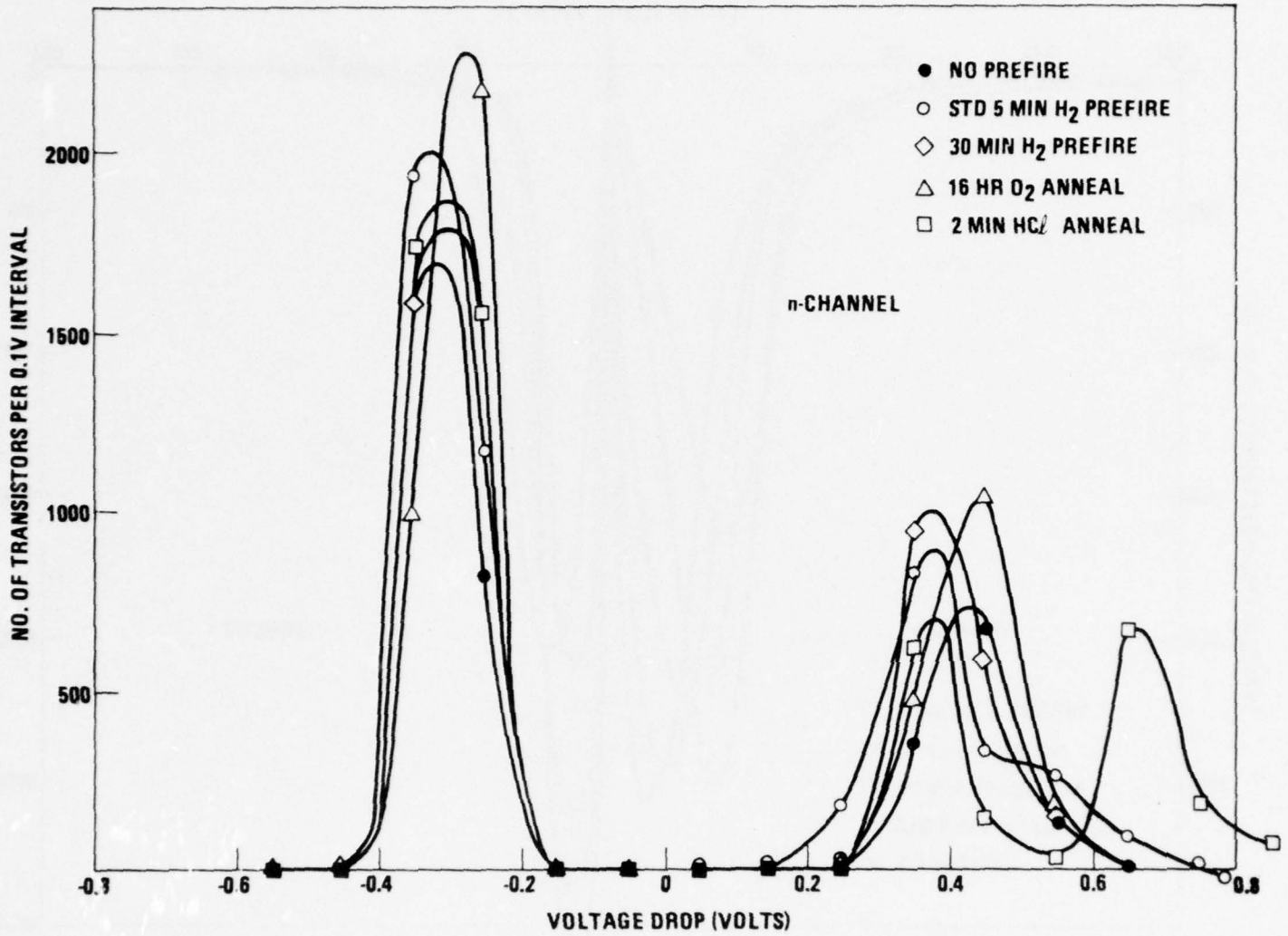

Figure 4-2. Effect of Pre-Epitaxial Anneal on Voltage Drop

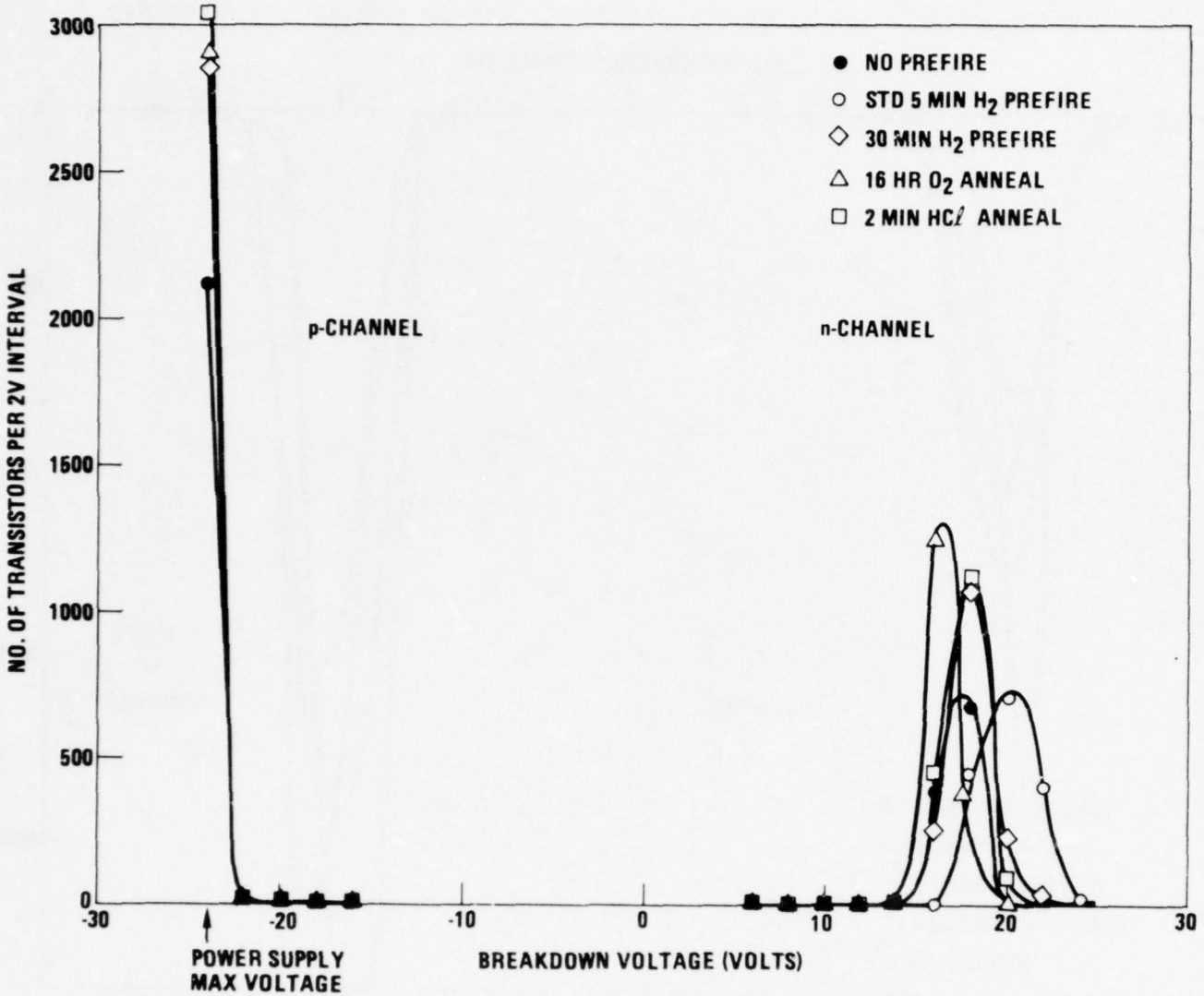

Figure 4-3. Effect of Pre-Epitaxial Anneal on Breakdown Voltage

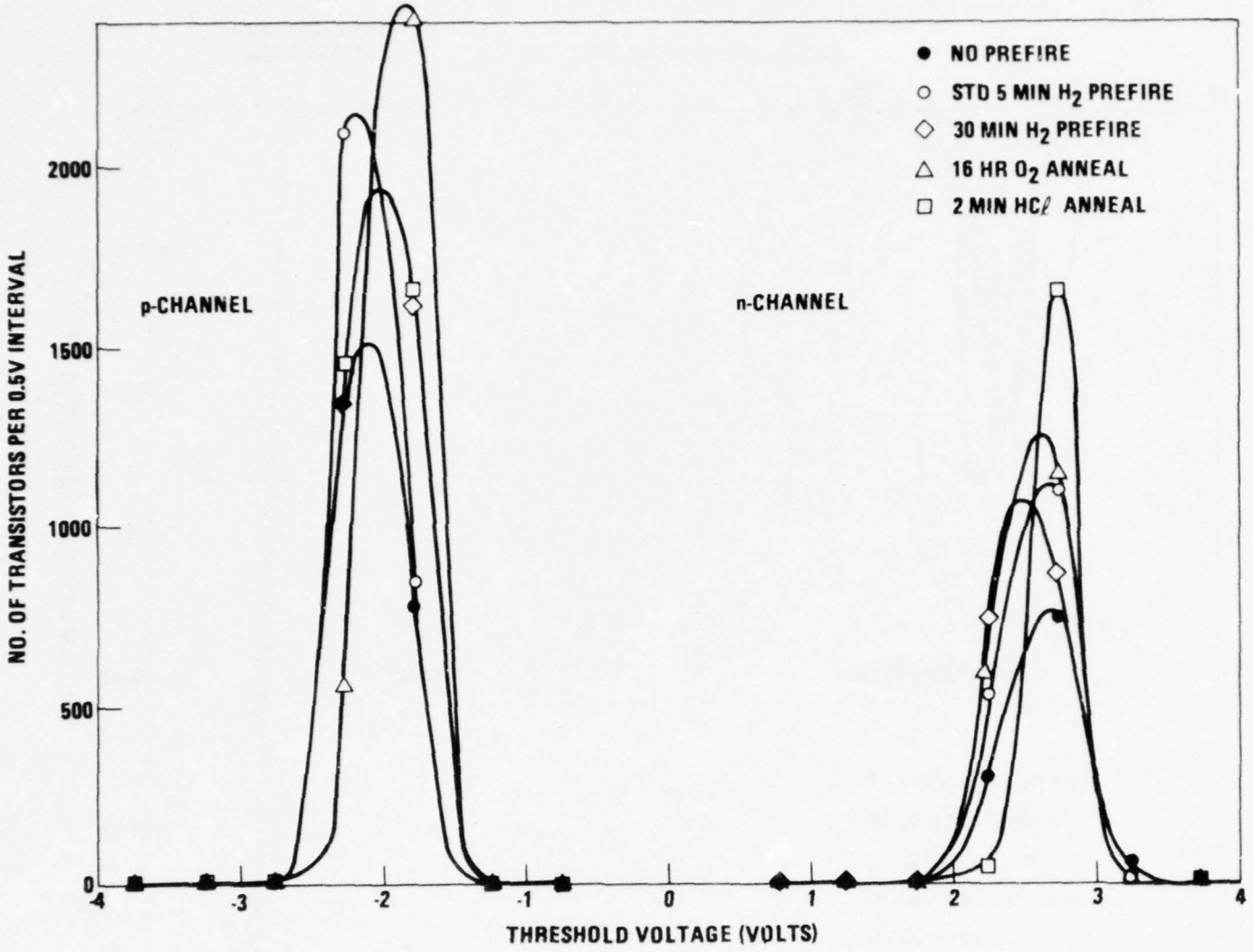

Figure 4-4. Effect of Pre-Epitaxial Anneal on Threshold Voltage

mapping and yield analysis of lot 627. This decision reflects the belief that the higher voltage drops were due to variations in device processing rather than to variations in wafer fabrication.

The wafer maps showed no significant local variations on any of the wafers, and were used only to identify good devices for radiation and bias-temperature testing. The yield analysis results are shown in Table 4-7. Due to the single inoperative n-channel device on every die (due to the faulty mask), there were no completely good dice on any of the wafers on lot 627. Hence, the comparison of pre-epitaxial annealing procedures must be based on inverter yields and yields of n- and p-channel transistors. In calculating inverter and n-channel yields, the single bad n-channel on every die was ignored. On this basis, it is apparent from the data of Table 4-7 that the wafers having no hydrogen prefire exhibited decidedly lower yields than the other wafers, the difference being a considerably higher number of n-channel leakage failures and a somewhat higher number of p-channel gate leakage failures. Of the other four pre-epitaxial anneal variations, only the HCl anneal is noticeably different from the others, giving a significant reduction in number of p-channel leakage failures.

Measurements of field-effect mobility were made at three locations on each wafer using the method outlined in Section C.4 of Appendix C. The results are shown in Table 4-8, where the average value of field-effect mobility for each wafer is listed for both n- and p-channel transistors. These values are in turn averaged for each group of wafers corresponding to a single annealing variation. The no-prefire case gives the lowest value of p-channel mobility and the highest n-channel mobility, while the 30-minute hydrogen prefire gives the lowest n-channel mobility and the second lowest p-channel mobility. The oxygen and HCl anneals both give high values for both n- and p-channel mobilities. In general, the p-channel mobilities in this lot (627) are lower than for the other lots. The difference between the field-effect mobilities obtained for the different pre-epitaxial annealing variations are not sufficiently large to have a significant effect on device performance.

4.6 Stability in Co^{60} Environment - Lot 627

The Co^{60} testing was done as described in Appendix D. The dice to be tested were selected on the basis of the wafer maps. Because the silicon film thickness was quite uniform on the wafers used in lot 627, and because of the large number of wafers in the lot, devices were taken only from one location near the center of each wafer to reduce test time. Radiation-induced threshold voltage shifts are shown in Table 4-9, where it is apparent that there is very little difference between the five pre-epitaxial anneal variations. One striking fact that was revealed by the conductance curves, however, was that devices from wafers 627.7

Table 4-7. Yield Results From Lot 627 - Pre-Epitaxial Annealing Variations
Numbers shown are numbers of failures.

PRE-EPITAXIAL ANNEAL	WAFER NUMBER	FAILED INVERTERS	FAILED p-CH	FAILED n-CH	p-CH LEAKAGE	n-CH LEAKAGE	p-CH VOLTAGE	n-CH VOLTAGE	p-CH GATE LEAKAGE	n-CH GATE LEAKAGE
No	627.1	304	236	284	162	265	2	0	74	19
Prefire	627.2	244	190	227	145	210	3	0	45	16
	627.11	196	106	180	56	171	0	1	50	9
	AVERAGE	41.3	19.7	38.4	13.4	35.9	0.19	0.06	6.3	2.4
	%									
Standard	627.9	228	171	193	146	173	1	0	25	19
5 Min	627.10	266	183	244	122	227	1	2	61	21
H_2	617.19	232	177	197	132	178	0	0	44	18
Prefire	627.20	166	112	146	77	131	0	5	35	17
	AVERAGE	37.2	17.9	32.5	13.3	29.5	0.06	0.29	4.6	3.1
	%									
30 Min	627.3	182	95	171	41	159	0	1	54	12
H_2	627.4	286	242	245	189	221	2	3	52	22
Prefire	627.13	165	121	143	82	130	2	0	39	13
	627.14	261	191	222	131	204	0	0	59	18
	AVERAGE	37.2	18	32.5	12.3	29.7	0.1	0.2	5.7	2.7
	%									
16 Hour	627.5	197	112	168	69	149	2	1	41	19
O_2	627.6	253	167	222	89	209	2	1	76	13
Anneal	627.15	281	221	238	176	212	0	1	45	25
	627.16	165	120	128	90	112	1	0	30	16
	AVERAGE	37	17	31.5	12	28	0.1	0.1	5	3
	%									
2 Min	627.7	158	56	149	34	81	1	62	22	10
$HC\ell$	627.8	211	110	192	68	182	1	0	42	9
Anneal	627.17	301	227	268	144	257	2	1	81	11
	627.18	197	93	181	56	116	0	54	37	14
	AVERAGE	36	13.5	33	8	26.5	0.1	49	5	1.8
	%									

Table 4-8. Effect of Pre-Epitaxial Annealing on Field-Effect Mobility

Pre-Epitaxial Anneal	Wafer Number	Average Field-Effect Mobility p-channel	n-channel
No Prefire	627.1	172.1	416.9
	627.2	172.8	424.0
	627.11	193.4	382.3
	Average	179.4	407.7
Standard 5 Minute H_2 Prefire	627.9	188.1	382.1
	627.10	194.5	388.9
	627.19	185.7	380.4
	627.20	192.1	371.5
	Average	190.1	380.7
30 Minute H_2 Prefire	627.3	195.9	389.7
	627.4	183.3	375.1
	627.13	184.9	385.0
	627.14	183.9	370.3
	Average	187.0	380.0
16 Hour O_2 Anneal	627.5	202.3	419.3
	627.6	196.4	395.6
	627.15	199.2	374.5
	627.16	190.3	414.6
	Average	197.1	401.0
2 Minute HCl Anneal	627.7	206.9	430.5
	627.8	191.1	393.7
	627.17	179.3	384.1
	627.18	197.1	406.7
	Average	193.6	403.8

Table 4-9. Effect of Pre-Epitaxial Anneal on Radiation-Induced Threshold Shift

Pre-Epitaxial Anneal	Wafer Number	n-Channel ΔV_T(Volts) $V_G = -10V$	n-Channel ΔV_T(Volts) $V_G = +10V$	p-Channel ΔV_T(Volts) $V_G = -10V$	p-Channel ΔV_T(Volts) $V_G = +10V$
No Prefire	627.1	-0.08	-0.47	-0.57	-2.19
	627.2	-0.10	-0.50	-0.60	-2.25
	627.11	-0.10	-0.35	-0.55	-1.97
	Average	-0.09	-0.44	-0.57	-2.14
Standard 5-Minute H_2 Prefire	627.9	-0.08	-0.67	-0.52	-2.15
	627.10	-0.09	-0.36	-0.61	-2.21
	627.19	-0.12	-0.42	-0.46	-1.95
	627.20	-0.10	-0.40	-0.47	-1.91
	Average	-0.10	-0.46	-0.515	-2.055
30-Minute H_2 Prefire	627.3	-0.10	-0.66	-0.59	-2.34
	627.4	-0.06	-0.36	-0.46	-1.93
	627.13	-0.09	-0.43	-0.54	-1.99
	627.14	-0.08	-0.50	-0.55	-2.13
	Average	-0.08	-0.49	-0.535	-2.10
16-Hour O_2 Anneal	627.5	-0.12	-0.35	-0.60	-2.16
	627.6	-0.11	-0.61	-0.55	-2.05
	627.15	-0.11	-0.66	-0.53	-2.25
	627.16	-0.12	-0.43	-0.55	-2.02
	Average	-0.115	-0.51	-0.56	-2.12
2-Minute HCl Anneal	627.7	-0.12	-0.67	-0.54	-2.05
	627.8	-0.08	-0.60	-0.50	-2.03
	627.17	-0.07	-0.60	-0.56	-2.12
	627.18	-0.10	-0.52	-0.47	-1.89
	Average	-0.09	-0.60	-0.52	-2.02

and 627.18 both showed a rapid decrease in n-channel transconductance for gate voltages above ~3.5 volts. This effect was not seen on any other wafers and accounts for the high voltage drops observed during wafer probing on n-channel transistors on wafers 627.7 and 627.18. The transconductance "roll-off" effect was not altered by the Co^{60} irradiation.

Radiation-induced leakage currents are shown in Table 4-10. Here the maximum leakage current, which always occurred under bias condition number 1, is shown, along with the ionizing radiation dose for which the maximum leakage was observed, and the initial thickness of the silicon film. As can be seen from Table 4-10, there is a wide wafer-to-wafer variation within the group of wafers for a given pre-epitaxial anneal procedure, but the variation between the averages for each procedure is not dramatic. Based on these averages, it appers that both the 0_2 and HCl annealing may be slightly detrimental to the goal of minimizing radiation-induced leakage, and that some hydrogen prefire is desirable, the lowest average leakage occurring with the 30-minute H_2 prefire. Finally, it should be noted that the rather large wafer-to-wafer variation is apparently not correlated with the silicon film thickness, but some correlation with the 1 through 10 and 11 through 20 processing split may be present.

4.7 Stability Under Bias-Temperature Stress - Lot 627

Due to the large number of wafers in this lot, this experiment was done on only one die from each wafer. The experiment was performed as outlined in Appendix E except that only the static bias conditions, 1 and 2, were used. This was done because only two inverter pairs were operational on each die in lot 627, and because the dynamic bias condition, 3, failed to produce any measurable change in design parameters in the previous B-T experiments. The results are summarized in Table 4-11. In all cases except one (627.14), threshold shifts were less than 0.35 volts, while in all cases but two (627.14 and 627.18), changes in maximum transconductance were less than 10%. It is of interest to note here that in most cases the transconductance was actually increased very slightly by the bias-temperature stress, whereas in previous experiments (Sections 2.6 and 3.6), the tendency was for the transconductance to decrease. In the case of leakage currents, in five cases (627.19, 627.20, 627.4, 627.14, and 627.16) there were large increases in drain leakage produced by the B-T stress.

Finally, no devices were rendered completely inoperative by the B-T stress, and in fact, some were actually improved, especially those from 627.7 and 627.18, where the rather extreme roll-off in transconductance observed initially was appreciably reduced by the B-T stress

Table 4-10. Effect of Pre-Epitaxial Anneal on Radiation-Induced Leakage Current

Pre-Epitaxial Anneal	Wafer Number	Device Number	Leakage Current (μA)	Dose (rads)	Si Thickness μm
No Prefire	627.1	2220	128	1×10^5	0.86
	627.2	1920	660	3×10^5	0.84
	627.11	1822	38	1×10^6	0.81
	Average		275		
Standard 5-Minute H_2 Prefire	627.9	1822	151	1×10^6	0.69
	627.10	1920	92	3×10^5	0.71
	627.19	2016	357	1×10^6	0.70
	627.20	1822	348	1×10^6	0.72
	Average		237		
30-Minute H_2 Prefire	627.3	1718	182	1×10^6	0.78
	627.4	2022	468	1×10^6	0.80
	627.13	1820	201	1×10^6	0.84
	627.14	2022	34	1×10^6	0.76
	Average		221		
16-Hour O_2 Anneal	627.5	2418	338	3×10^5	0.87
	627.6	1820	494	1×10^6	0.82
	627.15	1916	137	3×10^5	0.85
	627.16	2116	223	1×10^6	0.85
	Average		298		
2 Minute HCl Anneal	627.7	1918	192	3×10^5	0.78
	627.8	1916	418	1×10^6	0.79
	627.17	2020	605	1×10^6	0.75
	627.18	1918	67	1×10^6	0.80
	Average		320		

Table 4-11. Effect of Pre-Epitaxial Anneal on Bias-Temperature Stability

PRE-EPITAXIAL ANNEAL	WAFER NUMBER	DEVICE NUMBER	MAXIMUM THRESHOLD SHIFT			MAXIMUM TRANSCONDUCTANCE CHANGE			MAXIMUM DRAIN LEAKAGE		
			ΔV_T(VOLTS)	TYPE	BIAS	ΔG_M %	TYPE	BIAS	I_{DL}(μA)	TYPE	BIAS
No	627.1	1720	-0.2	P	2	0	–	–	0.06	P	2
Prefire	627.2	2420	-0.2	P	2	0	–	–	0	–	–
	627.11	1722	-0.27	N	1	0	–	–	0	–	–
Standard	627.9		-0.08	P	2	0	–	–	0	–	–
5 Min	627.10	1820	-0.18	P	2	0	–	–	0	–	–
H_2	617.19	2416	-0.20	P	2	0	–	–	140.3	P	1
Prefire	627.20	2122	-0.35	N	1	0	–	–	335	P	1
30 Min	627.3	2318	-0.20	P	2	0	–	–	0	–	–
H_2	627.4	2422	-0.06	P	2	0	–	–	150.8	P	1
Prefire	627.13	2120	-0.19	P	2	0	–	–	0	–	–
	627.14	1822	-1.8	N	1	-50	N	1	69.2	P	1
16 Hour	627.5	2416	-0.22	P	2	0	–	–	0	–	–
O_2	627.6	1420	-0.14	P	2	0	–	–	0	–	–
Anneal	627.15	2416	-0.10	P	2	+10	N	1	0	–	–
	627.16	1816	-0.3	N	1	0	–	–	35.5	P	1
2 Min	627.7	1818	-0.10	P	2	+10	N	2	0	–	–
$HC\ell$	627.8	2316	-0.06	P	2	0	–	–	0	–	–
Anneal	627.17	1820	-0.13	P	2	0	–	–	0.17	N	2
	627.18	2218	-0.19	P	2	+15	–	–	0	–	–

In general, the devices were so stable that no measurable change was induced by the B-T stress. It is believed that in those few cases where significant changes did occur, this could have been due to the choice of dice, giving results that may not have been characteristic of the whole wafer. The conclusion from these data is that all of the pre-epitaxial annealing procedures tried produced excellent bias-temperature stability.

4.8 Pre-Epitaxial Hydrogen Prefire and Annealing Results

The results of these experiments did not identify a preferred pre-epitaxial annealing procedure, but did indicate the desirability of having some hydrogen prefire.

The omission of the hydrogen prefire step produced a significant decrease in yield and perhaps some increase in radiation-induced leakage. Otherwise, differences between the results of the pre-epitaxial annealing variations were not significant, being much less than wafer-to-wafer variations within a group.

In general, the yields on this lot were lower than for lot 618 and approximately the same as yields measured for lot 610. However, the voltage drops were higher than in the previous lots, and the failure threshold for voltage drop under 3 mA load had to be raised to 0.8 V in order to pass most of the usable devices. Also, p-channel field-effect mobility tended to be lower and bias-temperature stability better, while radiation-induced leakage was higher than for the previous lots. These comments apply to all groups of wafers in this lot, including the four standard wafers which were part of the first shipment of wafers received from Union Carbide and used in lots 610 and 618. Thus, the differences between lot 627 and the two previous lots are believed to be processing related rather than starting-material related.

5. PHASE II SUMMARY, CONCLUSIONS AND RECOMMENDATIONS

The effect of pre-epitaxial treatments of sapphire on the quality of silicon-on-sapphire semiconductor material has been investigated to define improved procedures for fabricating SOS starting material. The pre-epitaxial treatments investigated were sapphire polishing, sapphire cleaning, and pre-epitaxial annealing. The quality of the resulting SOS material was assessed in terms of its suitability for the fabrication of radiation hard CMOS/SOS integrated circuits, as determined by evaluating CMOS devices fabricated in the SOS material. The devices used for the evaluation were 4007SR-H inverter circuits, and these were evaluated in terms of yield, electrical parameters, radiation tolerance, and stability under bias-temperature stress. The following conclusions were reached.

1. The reduction in final polishing time, from the standard Union Carbide procedure, provides a definite improvement in both n-channel yield and radiation-induced back-channel leakage, while having no measurable deleterious effects on either n- or p-channel transistors. This surprising conclusion is based on a very limited sample size, using repolished wafers which initially had the standard polish. Therefore, confirmation studies are required before any changes in standard polishing procedures could be recommended.

2. The radiation-induced back-channel leakage is very sensitive to silicon film thickness and can fall to ~0.2 μA/mil or below (after irradiation of up to 10^6 rads(Si) in a Co^{60} environment) when the film thickness is correct. This effect is believed to be due to the use of a deep boron implant on n-channels in order to increase the inversion potential of the back interface, and the correct silicon film thickness (about 0.8 μm for the process used here) is expected to depend upon the boron implant energy.

3. The use of alcohol in the final rinse during sapphire cleaning is detrimental to almost every investigated aspect of the devices. Although the use of an acid wash following an alcohol scrub removed the detrimental effects of the alcohol, other disadvantages were incurred, particularly in terms of survivability under bias-temperature stress.

4. The removal of detergents from the scrubbing cycle of the standard Union Carbide cleaning procedure may produce slight advantages in terms of field-effect mobility and bias-temperature stability.

5. Some hydrogen prefire is desirable, both from the point of view of device yield and radiation-induced n-channel leakage. Other pre-epitaxial annealing variations had no significant effect.

6. The principal factor in both yield and radiation hardness was n-channel leakage. The differences between the results of the different polishing, cleaning, and annealing procedures in terms of yield and radiation hardness are reflected almost entirely in the n-channel leakage results.

The first conclusion (number 1, above) is also supported by results obtained in Phase I. In view of these conclusions, the most promising areas for SOS film improvement appear to be sapphire polishing and silicon film thickness uniformity. Further, it is believed that it is not simply the sapphire polish which requires further study, but, in fact, all procedures used to determine the mechanical properties, including crystallographic orientation, of the sapphire surface. Similarly, it is not simply silicon film thickness uniformity which requires work, but in fact, all procedures which determine the boron doping level in the vicinity of the silicon-sapphire interface, including both the boron implantation procedure and the duration and temperature of subsequent high-temperature processing steps. Thus it may be more fruitful to attempt to develop an implantation process which is not sensitive to the 10% to 15% silicon thickness variation seen across a typical SOS wafer than to attempt to develop a silicon epi procedure which yields very uniform silicon film.

Although the total number of devices measured was extremely large ($\sim 7 \times 10^4$), the number of wafers per variation was very small (≤ 4). Since the wafer-to-wafer variations were relatively large, the statistics on a wafer-to-wafer basis are dominant. Thus a larger number of wafers per variation would be desirable for future investigations, although there will always be the limitations of wafer-processing lot size. Since differences in results observed for different processing lots is quite large, a large number of processing runs is also desirable.

Although it has not been possible to obtain excellent statistics on this study program, the consistency of many of the results is very good. For example, in the area of device yield, on lot 627 the yield results for all the pre-epitaxial anneal variations are virtually identical, except for the wafers where no hydrogen prefire was used (see Table 4-7).

Finally, it must be noted that the present studies all used a particular process designed to produce radiation-hard CMOS/SOS devices. The results obtained, therefore, derive from the interaction of the device processing with the SOS material and might, therefore, be different for different processes. This is probably particularly true of the effects of nonuniform silicon thickness on radiation-induced n-channel leakage. Therefore, only to the extent that the present process is typical of other radiation-hard CMOS/SOS processes or to the extent that the interactions between processes and SOS material are understood, can the results described in this report be applied in general to radiation-hard CMOS/SOS device fabrication.

APPENDIX A

WAFER INSPECTION TECHNIQUES

This appendix describes the techniques used in the study to characterize SOS starting-material wafers prior to the start of CMOS/SOS wafer processing.

A.1 Sodium Light Interferometer

Topographs of the silicon films on the SOS wafers used in the study were obtained by making photomacrographs of the wafers under monochromatic sodium light (wavelength, λ = 5893 Å).

Variations in the silicon film thickness, as shown in Figure A1, are revealed by interference fringes which result from the incident beam and the light transmitted through the silicon and reflected from the sapphire surface.

Because the sodium light topographs were made after the island etch, it was possible to establish permanent row and column identification numbers for the devices (see Appendix C, Figure C1) and to correlate test results on subsequently fabricated devices with their relative silicon thicknesses.

A.2 Nomarski Interference Contrast Filter

The Nomarski interference contrast filter* permits differential surface analysis where surface variations are so slight that they are not revealed by the usual optical techniques.

The Nomarski filter is placed between the illuminator and the objective of an incident-light microscope having a polarizer-analyzer, as shown in Figure A2. A modified Wollaston prism splits the light from the sample into two superimposed images that are slightly displaced from one another giving the desired three-dimensional effect.

A.3 Infrared (IR) Spectrophotometer

The Beckman IR-5A spectrophotometer used in the experiments consists of an IR radiation source and a monochromator containing a prism which disperses the light so that a limited wavelength range is allowed to irradiate the SOS sample. The light reflected from the wafer is detected by a photodetector, the output of which is used to drive a strip-chart recorder.

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*G. Nomarski and A. R. Weill, Rev. DeMétallurgie, 1955.

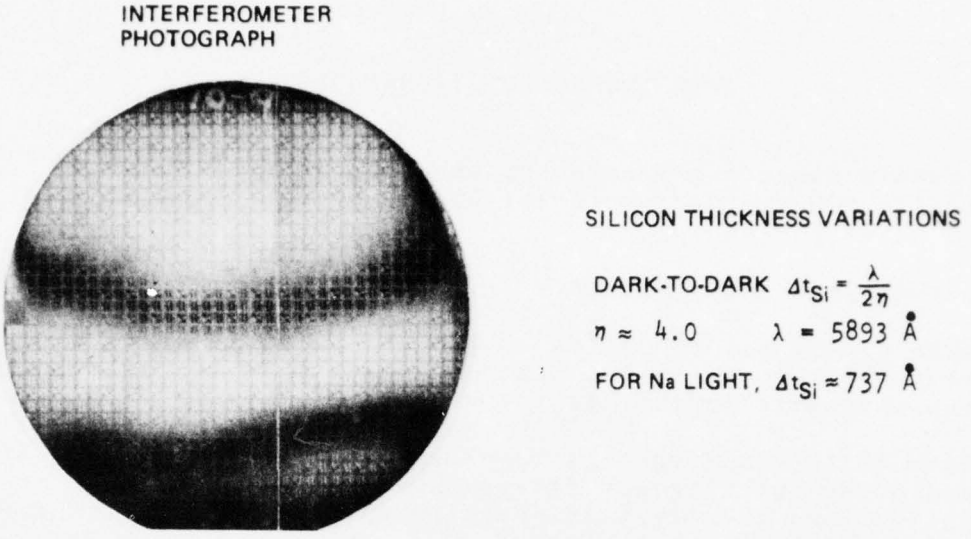


Figure A1. Interferometer Measurement of Silicon Thickness Uniformity

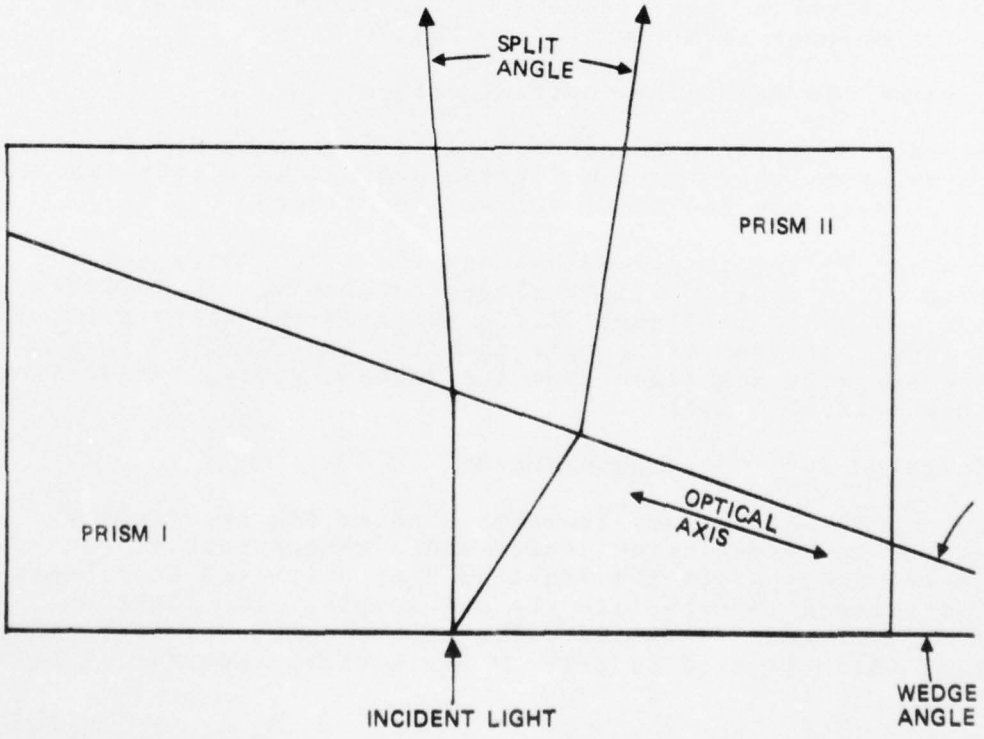
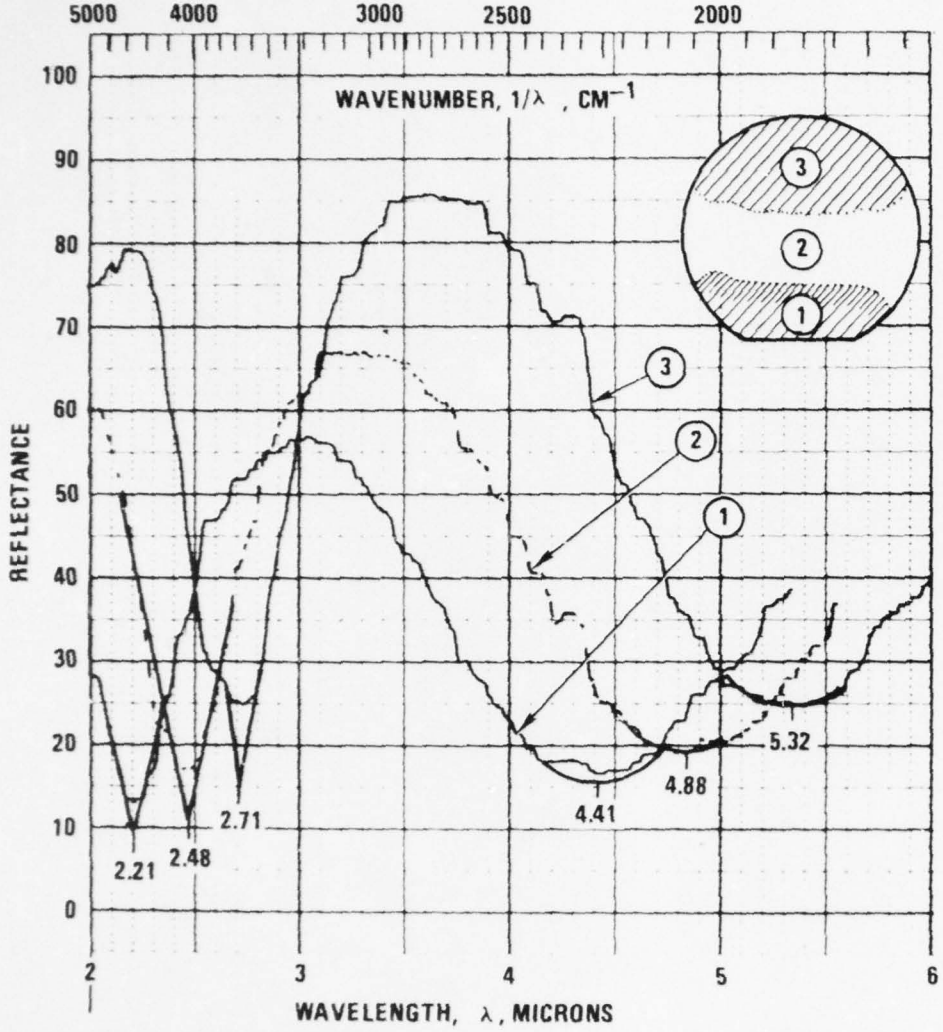


Figure A2. Nomarski Interference Contrast Filter; Modified Wollaston Prism Which Provides a Three-Dimensional Effect

Figure A3 shows the detector output traces for three locations on one SOS wafer, and the equation used to calculate the silicon thickness. This technique, coupled with the sodium light topograph, provides a quick visual indication of silicon film thickness variations on SOS wafers.



MEASUREMENT NUMBER	MICRONS		
	λ_1	λ_2	t_{si}
①	2.21	4.41	0.648
②	2.48	4.83	0.745
③	2.71	5.32	0.808

$$t_{Si} = \frac{N}{2\sqrt{\eta^2 - \mathrm{Sin}^2\theta}} \left[\frac{\lambda_1 \quad \lambda_2}{\lambda_2 - \lambda_1}\right]$$

N = NUMBER OF WAVELENGTH ORDERS
η = 3.42 = INDEX OF REFRACTION OF SILICON RELATIVE TO AIR.

FOR OUR MEASUREMENTS, N = 1 AND $\theta = 0^0$

$$t_{Si} = \frac{1}{2\eta} \left[\frac{\lambda_1 \quad \lambda_2}{\lambda_2 - \lambda_1}\right]$$

Figure A3. IR Spectrophotometer Measurement of Silicon Thickness

APPENDIX B

CMOS/SOS DEVICE FABRICATION

A simple, metal gate process which exhibits excellent electrical characteristics, radiation hardness and bias-temperature stability was used to fabricate devices on the SOS samples. A 4007SR test vehicle comprised of a basic dual complementary pair plus inverter circuit (CD4007 equivalent) and special test structures was chosen for fabrication using the following process sequence:

1. The silicon islands were formed by first oxidizing the silicon surface in a steam ambient followed by a drying cycle. The islands were defined by standard photolithographic techniques, and the oxide was etched in a buffered HF solution. Following the oxide etch, the photoresist was removed and the silicon was etched in a KOH solution.

2. A thin thermal oxide was grown on the silicon islands followed by a deposition of Silox. The source and drain region of the n-channel transistors was then defined with photoresist, and the oxide was etched to silicon. The N^+ regions were then doped using $POCl_3$ as the source.

3. The wafers were then oxidized to form an oxide over the N^+ regions. The p-channel transistor source-drain areas were then defined with photoresist, and the oxide was etched to silicon. Following the removal of the photoresist, the P^+ regions were doped using boron nitride wafers as a doping source. All oxide was then removed followed by a short thermal oxidation.

4. The p-well was then defined using photoresist as an implantation mask. The p-well was ion implanted at 200 keV to a dose of 1.5×10^{13} atoms/cm^2 and 40 keV to a dose of 3×10^{12} atoms/cm^2. The diffusions were then driven at 1000°C for two hours.

5. All oxide was stripped. The gate oxide was then grown in a steam ambient with ~1% HCl present at 875°C and annealed at 875°C in dry nitrogen.

6. The contacts were defined by photoresist and etched.

7. Metallization was deposited using an AMT Insource 1500 RF evaporation system. The metal was defined using photoresist and etched. Following photoresist removal, the wafers were sintered.

8. Finally, a Silox overcoat was deposited and the bonding and probe pads were opened using standard photolithographic techniques.

APPENDIX C

WAFER PROBING-DATA ACQUISITION AND ANALYSIS

C.1 Data Acquisition

Following device fabrication, the wafers were probed on an automatic wafer probing setup controlled by a Hewlett Packard 2114B mini-computer. A program was written to probe the 4007-H inverters, measuring the following parameters on each transistor: (1) drain junction leakage current (channel leakage) with the drain junction reverse biased at 10 V and with the gate grounded, (2) voltage drop at 3 mA load with the gate biased strongly on ($|V_{GS}|$ = 10 V), (3) gate leakage current with 12 volts applied between the gate and the source, (4) gate leakage current with 12 volts applied between the gate and both drain and source, (5) drain junction breakdown voltage with 10 μA through the back-biased drain junction, (6) turn-on threshold voltage, taken by measuring the gate to source voltage produced by forcing 100 μA through the back-biased drain junction with the gate tied to the drain. The measurements were done on each transistor in the order outlined above. If any of the first four measurements exceeded certain limits, the remaining measurements on the device were aborted and the next device was tested. These limits were 100 nA for the drain leakage, 2 volts for the voltage drop, and 1 μA for the gate leakages.

Rather than probing all the devices on a wafer, in order to speed up the probing process and to facilitate completely automatic probing, only the dice within a square area inscribed in the circular wafer were probed. Because alternate dice along every other row were special ten-pad test devices rather than 4007-H inverters, only alternate dice were probed on every row. Thus the probing was done on 12 dice on each of 25 rows, giving a total of 300 dice probed, including 900 inverters consisting of 900 n-channel and 900 p-channel transistors. The probed area is illustrated in Figure C1. This scheme allowed the probing operation to be completely automatic and quite rapid, so that after the probe was started at the upper left-hand corner of the area to be probed, the operation proceeded without requiring any attention from the operator until the 300 dice had been probed about 3-1/2 hours later. The data were stored on magnetic tape and were then analyzed by other computer programs written for the mini-computer.

C.2 Wafer Mapping

Device failures were mapped for the square, probed area of each wafer, using the device measurements stored on the magnetic tape. Mapping was done on one row at a time by reading the data for the 12 dice on a row into the computer from the magnetic tape, and comparing the values of the drain junction leakage current,

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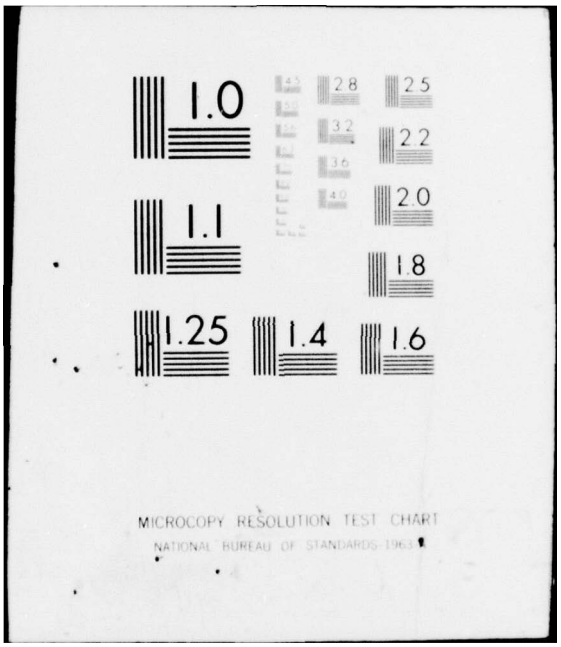
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1.1
1.25
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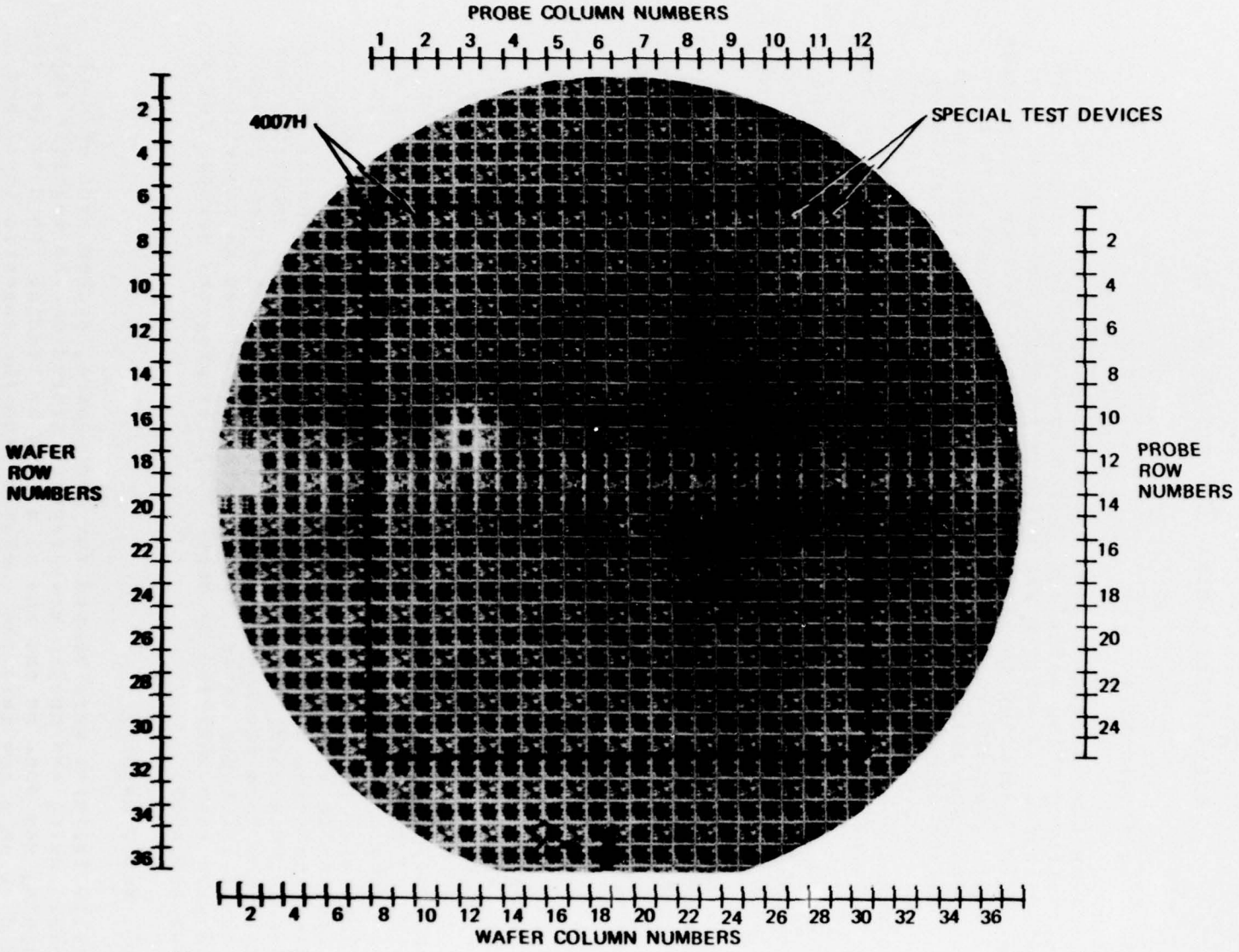


Figure C1. Probed Area of Wafer Processed With 13001 Mask Set

voltage drop, and gate leakage current with failure threshold values. The failure threshold values were read-in at the beginning of each mapping operation and were ordinarily chosen to be 100 nA for drain leakage, 0.5 V for voltage drop, and 1 μA for gate leakage. If a device passed all four comparisons, a zero was printed as its position within the die at the proper die location within the row. If a device failed one of the comparisons, then subsequent comparisons for the device were aborted and a number between 1 and 4, corresponding to the test failed, was printed in the position corresponding to that device. Thus the number 1 corresponds to drain leakage failure, 2 to voltage drop, and 3 and 4 to gate leakage.

In addition to mapping the failures, the computer program kept track of the total numbers of failures of various types and, after all 25 rows had been mapped, the number of die containing one or more failed devices, number of failed inverters, number of failed n-channel transistors, number of failed p-channel transistors, plus numbers of n-channel and p-channel transistors failing each of the four tests was printed. A typical mapping and yield analysis result is shown in Figure C2. Individual dice are outlined on this figure, and the first test number failed for each of the three n-channel and three p-channel transistors is shown within each die, with the n-channels on the left and the p-channels on the right. The yield analysis results appear below the map. It should be noted that devices failing the drain leakage test are automatically recorded as also failing the voltage drop and gate leakage tests.

C.3 Parameter Distributions

The wafer probe measurements, stored on the magnetic tape cassette, were read into the computer and sorted into ten ranges for each parameter. The ranges for leakage current were from 0 to 200 nA in steps of 20 nA, for voltage drop were from 0 to 1 volt in steps of 0.1 V, for gate leakage were from 0 to 2 μA in steps of 0.2 μA, for breakdown voltage were from 5 to 25 volts in steps of 2 volts, and for threshold voltage were from 0.5 to 5.5 volts in steps of 0.5 volts. In addition, the number of devices falling above the sorted range and the number of devices not tested were determined for each type of measurement. A typical result is shown in Figure C3. The test numbers, 1 through 6, on this figure correspond to the measurements in the order performed--namely, (1) drain leakage, (2) voltage drop, (3) gate-to-source leakage, (4) gate-to-drain and source leakage, (5) drain breakdown voltage, and (6) turn-on threshold voltage.

C.4 Field-Effect Mobility Measurements

These measurements are made on the special test dice located between 4007SR dice on alternate rows of the wafer. The test is made under the control of the mini-computer using the automatic probe table in the manual mode. The computer obtains measurements of channel current versus gate voltage using 0.5 V gate

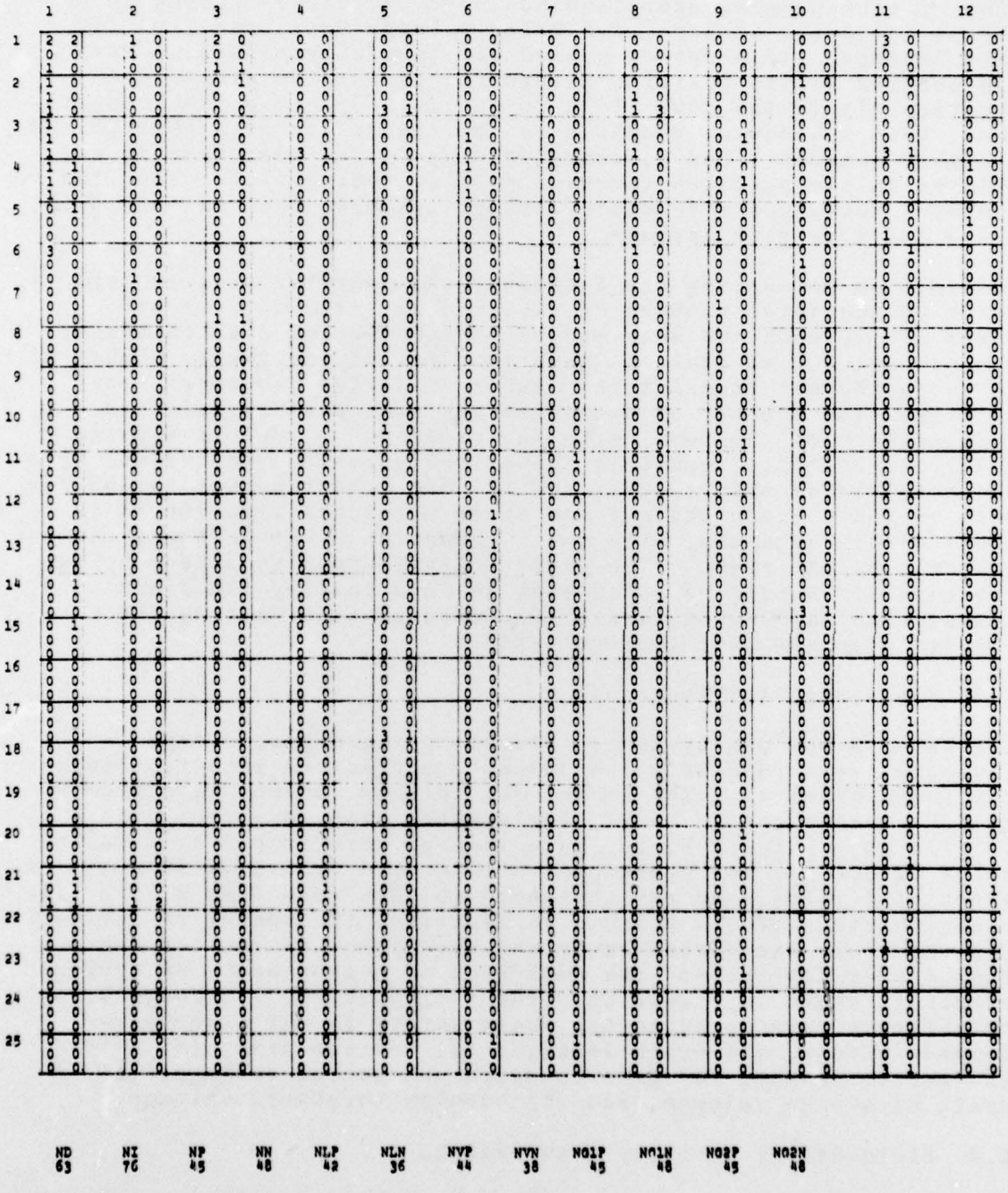


Figure C2. Wafer Map and Yield Analysis for Wafer 618.8. Numbers at the top of the page are failure threshold assignments for drain leakage, voltage drop, and both types of gate leakage.

WAFER SUMMARY

TEST NO. 1 UNITS .1E-08

RANGE	.00	20.00	40.00	60.00	80.00	100.00	120.00	140.00	160.00	180.00	200.00	NO TEST
N CHANNEL	2	175	618	60	9	6	4	2	3	1	20	0
P CHANNEL	678	163	11	4	2	0	1	0	1	1	38	1

TEST NO. 2 UNITS 1.0E+00

RANGE	.00	.10	.20	.30	.40	.50	.60	.70	.80	.90	1.00	NO TEST
N CHANNEL	0	851	10	1	0	0	0	0	0	0	1	37
P CHANNEL	0	0	856	0	0	1	0	0	0	0	0	43

TEST NO. 3 UNITS 1.0E-06

RANGE	.00	.20	.40	.60	.80	1.00	1.20	1.40	1.60	1.80	2.00	NO TEST
N CHANNEL	844	4	2	2	0	1	2	1	0	1	6	37
P CHANNEL	847	2	2	1	2	0	0	0	0	0	2	44

TEST NO. 4 UNITS 1.0E-06

RANGE	.00	.20	.40	.60	.80	1.00	1.20	1.40	1.60	1.80	2.00	NO TEST
N CHANNEL	845	3	2	2	0	1	3	0	0	1	6	37
P CHANNEL	846	2	3	1	1	0	0	0	0	0	2	45

TEST NO. 5 UNITS 1.0E+00

RANGE	5.00	7.00	9.00	11.00	13.00	15.00	17.00	19.00	21.00	23.00	25.00	NO TEST
N CHANNEL	0	0	0	0	6	539	307	0	0	0	0	48
P CHANNEL	0	0	0	0	1	0	0	1	3	849	0	46

TEST NO. 6 UNITS 1.0E+00

RANGE	.50	1.00	1.50	2.00	2.50	3.00	3.50	4.00	4.50	5.00	5.50	NO TEST
N CHANNEL	0	0	270	578	0	0	0	0	0	0	0	52
P CHANNEL	0	0	855	0	0	0	0	0	0	0	0	45

Figure C3. Parameter Distributions for Wafer 618.8. Test numbers refer to the following measurements: 1 → I_{DL}, 2 → V_{DS}, 3 & 4 → I_{GL}, 5 → V_{BD}, 6 → V_T.

voltage steps and with the drain biased at 0.1 V. The computer then selects the region of maximum transconductance ($\delta I_D / \delta V_G$) from these points and determines the field-effect mobility from the formula

$$\left.\frac{\delta I_D}{\delta V_G}\right|_{max} = \frac{Z}{L} \mu_{FE} C_o V_D$$

Where Z/L is the channel width-to-length ratio, μ_{FE} is the field-effect mobility, C_o is the oxide capacitance per unit area, and V_D is the drain voltage. The oxide capacitance was obtained from measurements of minimum and maximum gate capacitance of a 4 mil x 4 mil transistor on the special test dice. From these measurements, both oxide thickness and substrate doping were obtained. The oxide capacitance was then calculated from the oxide thickness.

APPENDIX D

CHARACTERIZATION IN Co^{60} ENVIRONMENT

Devices representative of the fabricated wafers were characterized prior to and following Co^{60} exposure under various bias conditions. The primary purpose of these experiments was to determine the gate oxide radiation hardness by monitoring the shifts in threshold voltage and to determine the hardness of the silicon-sapphire interface by measuring the increases in drain leakage current with increasing ionizing radiation dose. The dice selected for radiation testing were chosen on the basis of the wafer mapping and the silicon film thickness measurements. Six dice containing at least two fully functional complementary pairs were taken from three locations covering the range of film thicknesses present on the wafer.

The threshold shift data were obtained from shifts in conductance versus gate voltage curves. The conductance measurements were made on each transistor with the source at 0.1 volt, the drain connected to the input of an operational amplifier, and the gate swept with a positive or negative ramp. The output of the operational amplifier was used to drive the vertical Y axis of an X-Y recorder, while the ramp used to sweep the gate was connected to the horizontal X axis.

The drain junction leakage measurement was made by grounding the gate and source and measuring the current in the drain using a Fluke Digital Multimeter with +10 volts on the drain for the n-channel and -10 volts on the drain for the p-channel devices, as illustrated in Figure D1. Also gate leakage measurements were made by

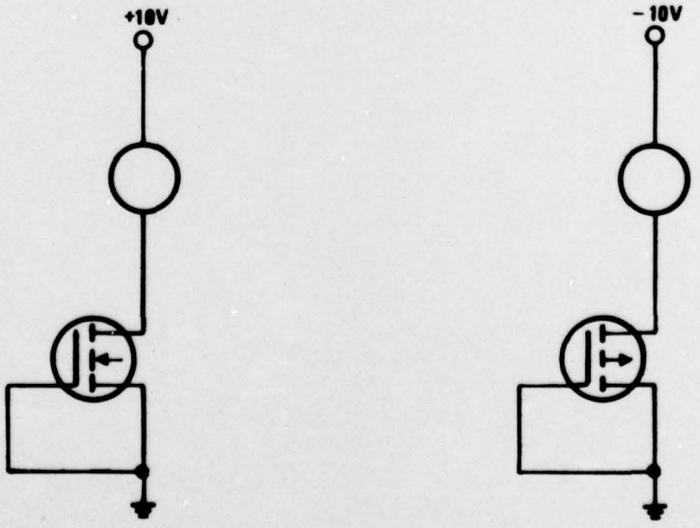
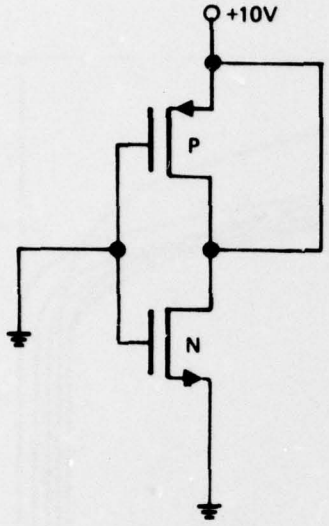


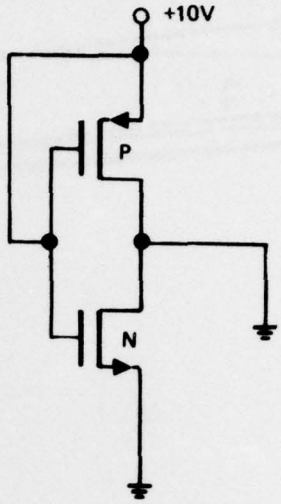
Figure D1. Drain Leakage Measurement

apply 10 volts between the gate and source with zero drain bias and measuring the current into the gate with a Fluke Digital Multimeter.

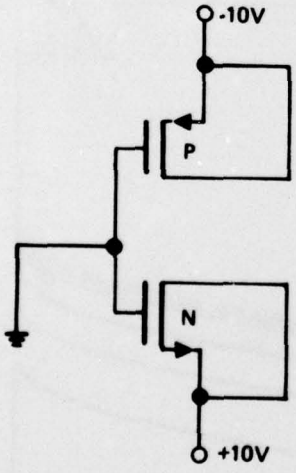
Two dice from each wafer location were irradiated with each of the four complementary pairs in a different one of the four bias conditions illustrated in Figure D2. The four bias conditions provide a positive and negative gate bias condition for a zero drain bias condition plus a zero gate bias for both a zero and 10 volt drain bias condition for each transistor. The three measurements--conductance, drain junction leakage, and gate leakage--were made prior to the first irradiation and after a series of radiation doses (.01, .03, .1, .3, and 1 megarad). A typical set of conductance results for one of the four bias conditions is shown in Figure D3. Under this bias condition, the n-channel is seen to develop leakage during irradiation. The leakage currents measured under 10 volt drain bias usually behaved in a similar manner with radiation dose as the 0.1 volt conductance measurement. After noting cases in lot 618 where the 10 volt and 0.1 volt n-channel leakage behavior with radiation dose did not correspond well, a leakage characteristic curve was also generated on subsequent tests by sweeping the n-channel drain between zero and +10 volts with the gate held at -10 volts.



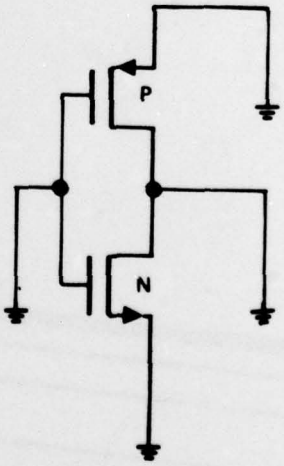
(1) P-ch V_{GS} = -10V V_{DS} = 0
N-ch V_{GS} = 0 V_{DS} = +10V



(2) P-ch V_{GS} = 0 V_{DS} = -10V
N-ch V_{GS} = +10V V_{DS} = 0



(3) P-ch V_{GS} = +10V V_{DS} = 0
N-ch V_{GS} = -10V V_{DS} = 0



(4) P-ch V_{GS} = 0 V_{DS} = 0
N-ch V_{GS} = 0 V_{DS} = 0

Figure D2. Bias Conditions Used During Co^{60} Irradiation

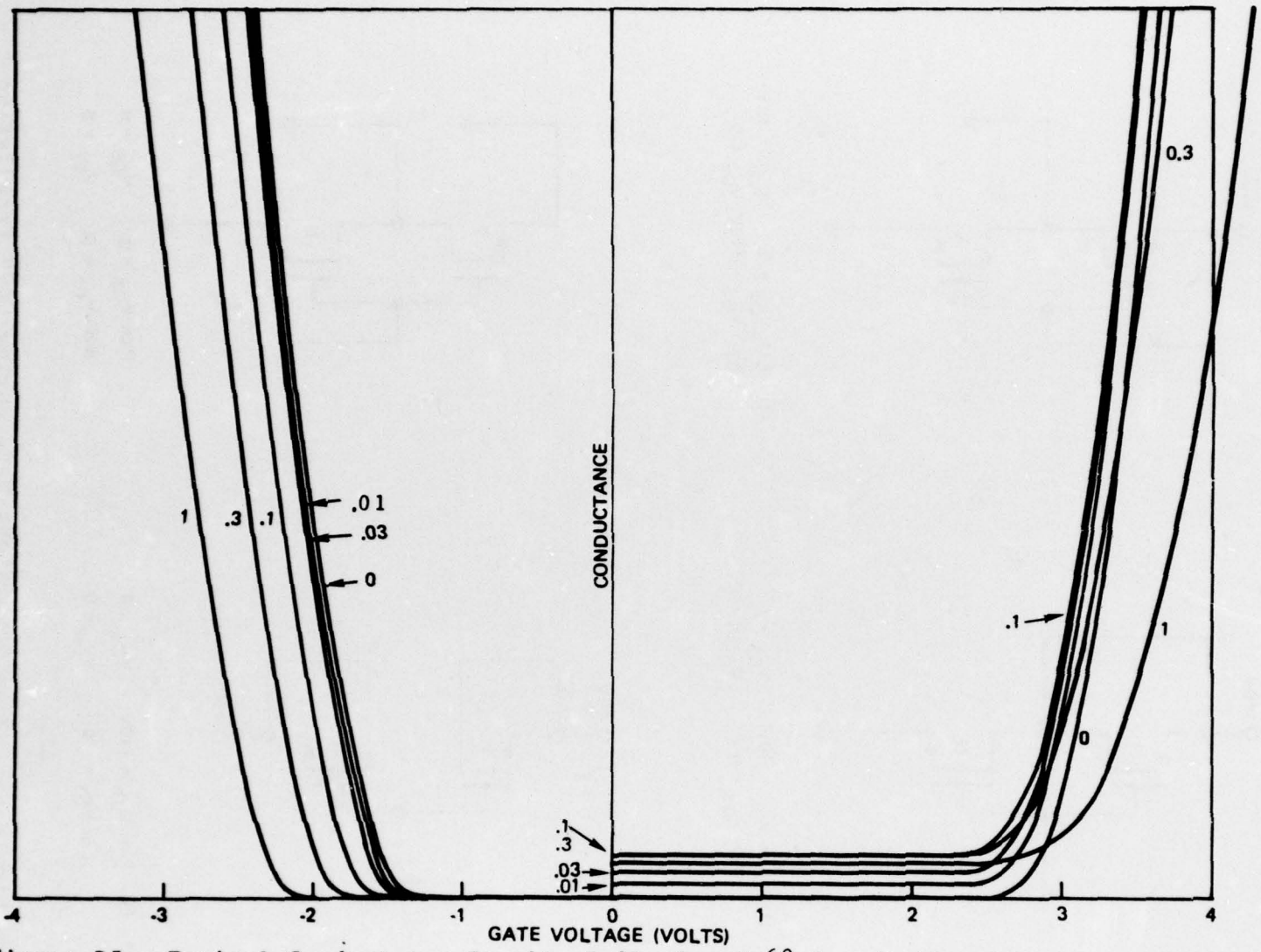
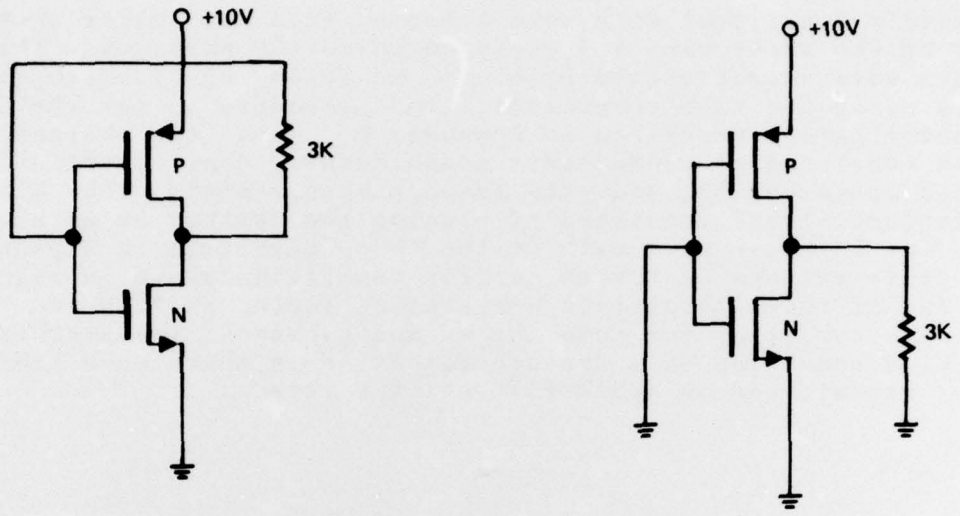


Figure D3. Typical Conductance Results Following Co^{60} Irradiation. Curves are Labeled With Radiation Dose in Megarads

APPENDIX E

BIAS-TEMPERATURE CHARACTERIZATION

Completely functional dice were selected from each wafer on the basis of the wafer maps and packaged in TO-100 packages. The devices were characterized prior to and following bias temperature stress using the same characterization procedure as for the Co^{60} characterization described in Appendix D. Thus, the characterization consisted of conductance measurements, drain junction leakage measurements, and gate leakage measurements. The bias-temperature stress consisted of placing the devices in an oven at 260°C for 16 hours with each of the three inverters in a package in a different one of the three bias conditions shown in Figure E1. Two of these conditions are static, giving an "on" and "off" gate bias condition for both the n- and p-channel transistors. The third condition is a dynamic condition in which each transistor is switched on and off at a 1 MHz rate.



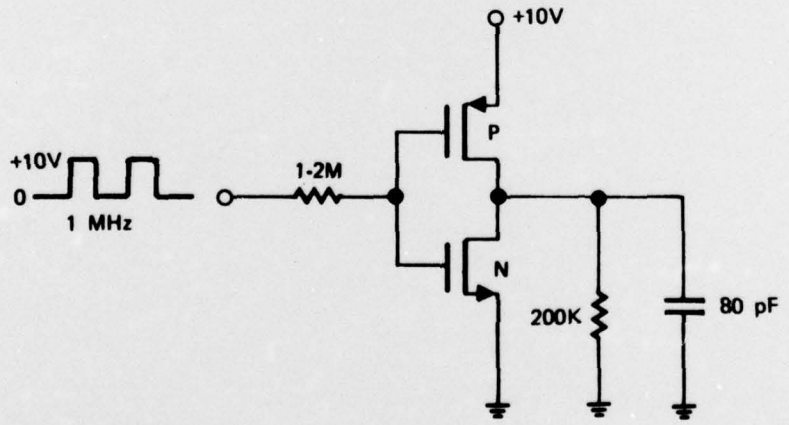


Figure E1. Inverter Bias Conditions During Bias-Temperature Stress

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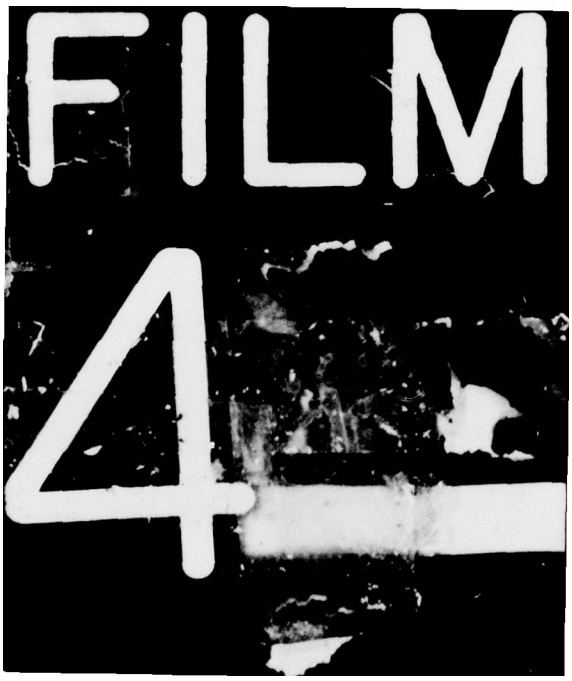
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